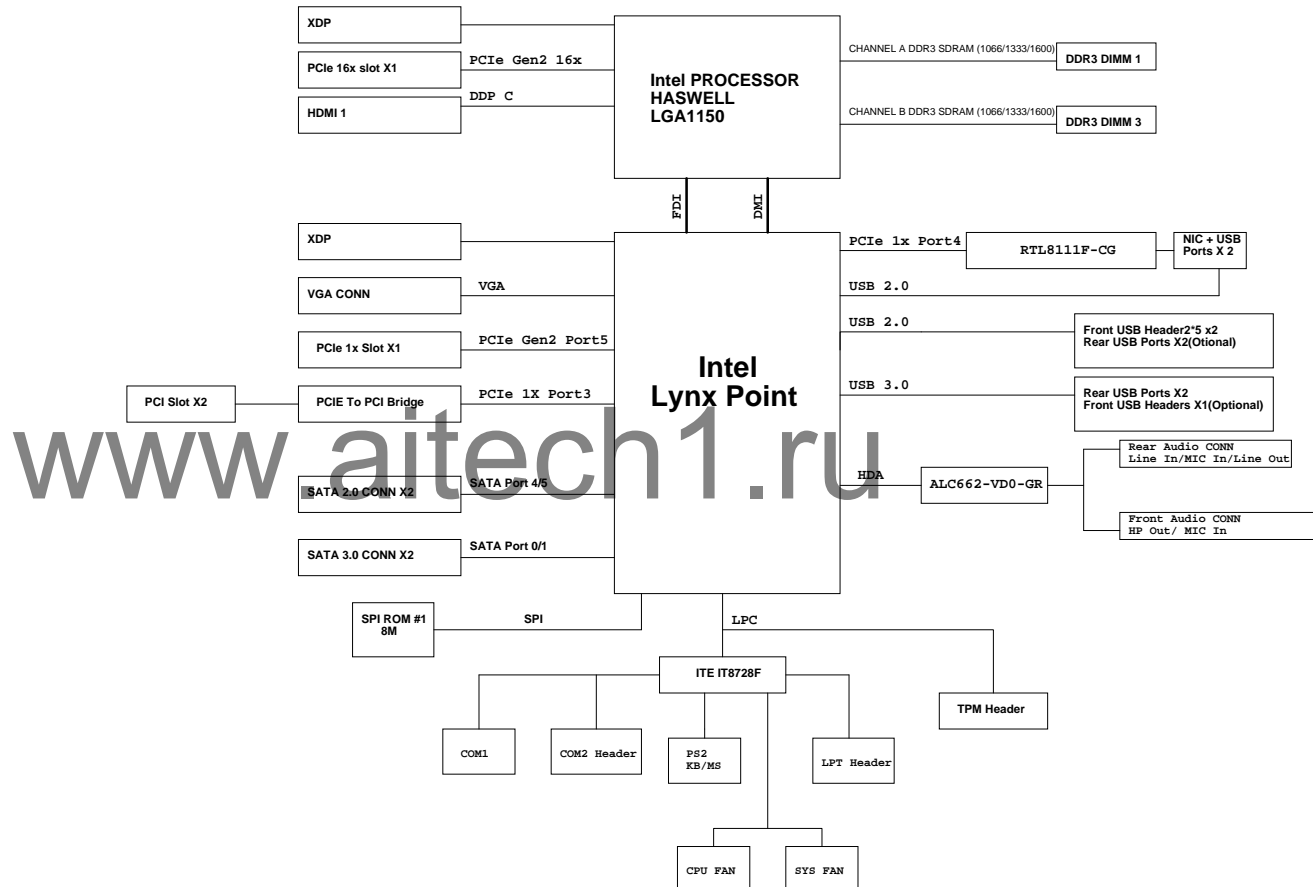


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FAB:A

1. Index / Block diagram
2. SMBus MAP
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26. PCIE TO PCI BRIDGE
27. PCI SLOT X2
28. LAN_RTL8111F
29. USB 3.0
30. USB 2.0
31. AUDIO ALC662
32. AUDIO CONN/HEADER
33. SPI_Socket_ROM
34. SIO-IT8728
35. PS2/COM/LPT
36. FAN/TPM
37. ATX CONN/FP PANEL/EMI PART
38. Linear Power
39. 1.05V_PCH
40. 5V_DUAL/3D3V_DUAL
41. V_SM
42. Vcore PWM
43. Vcore Driver

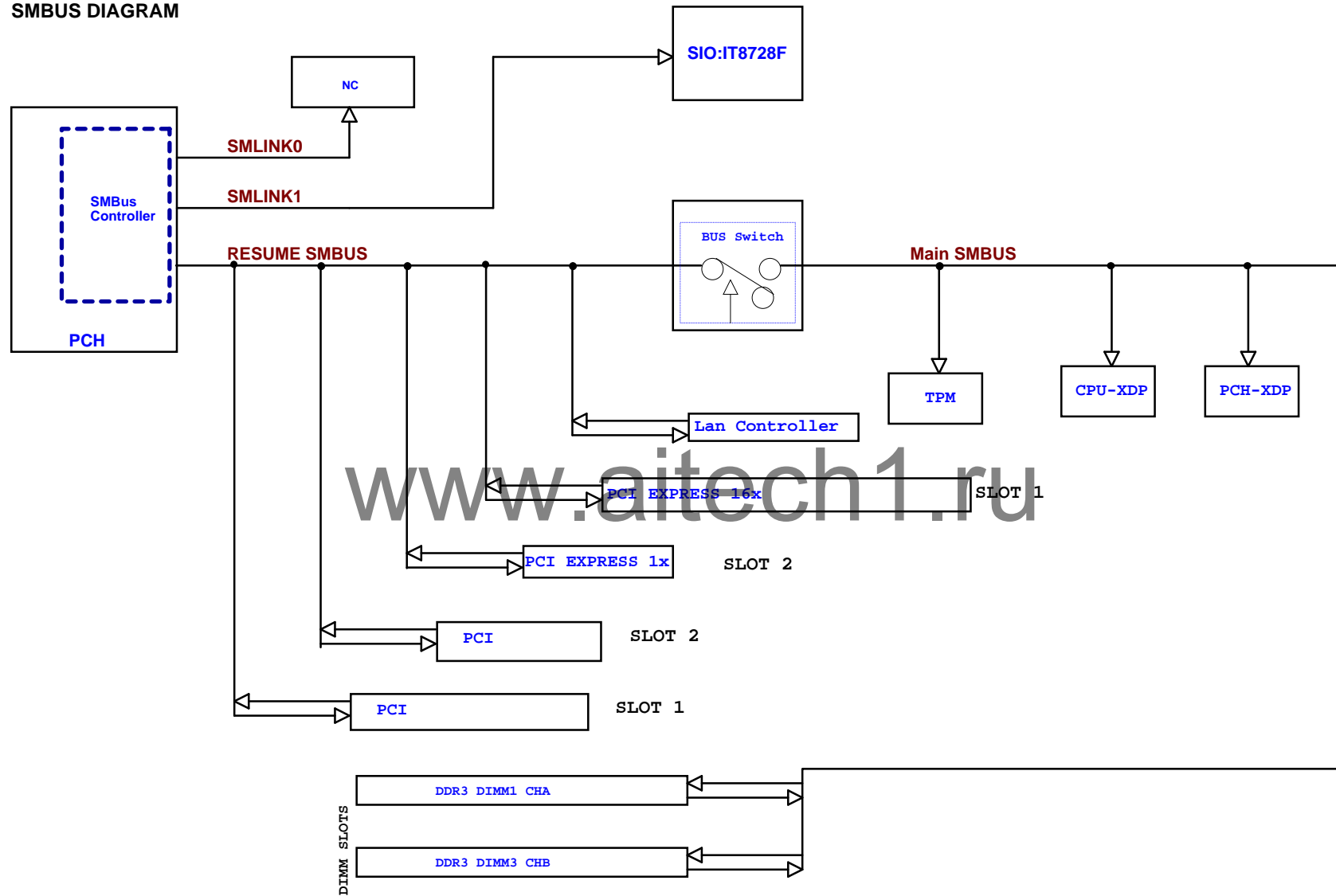


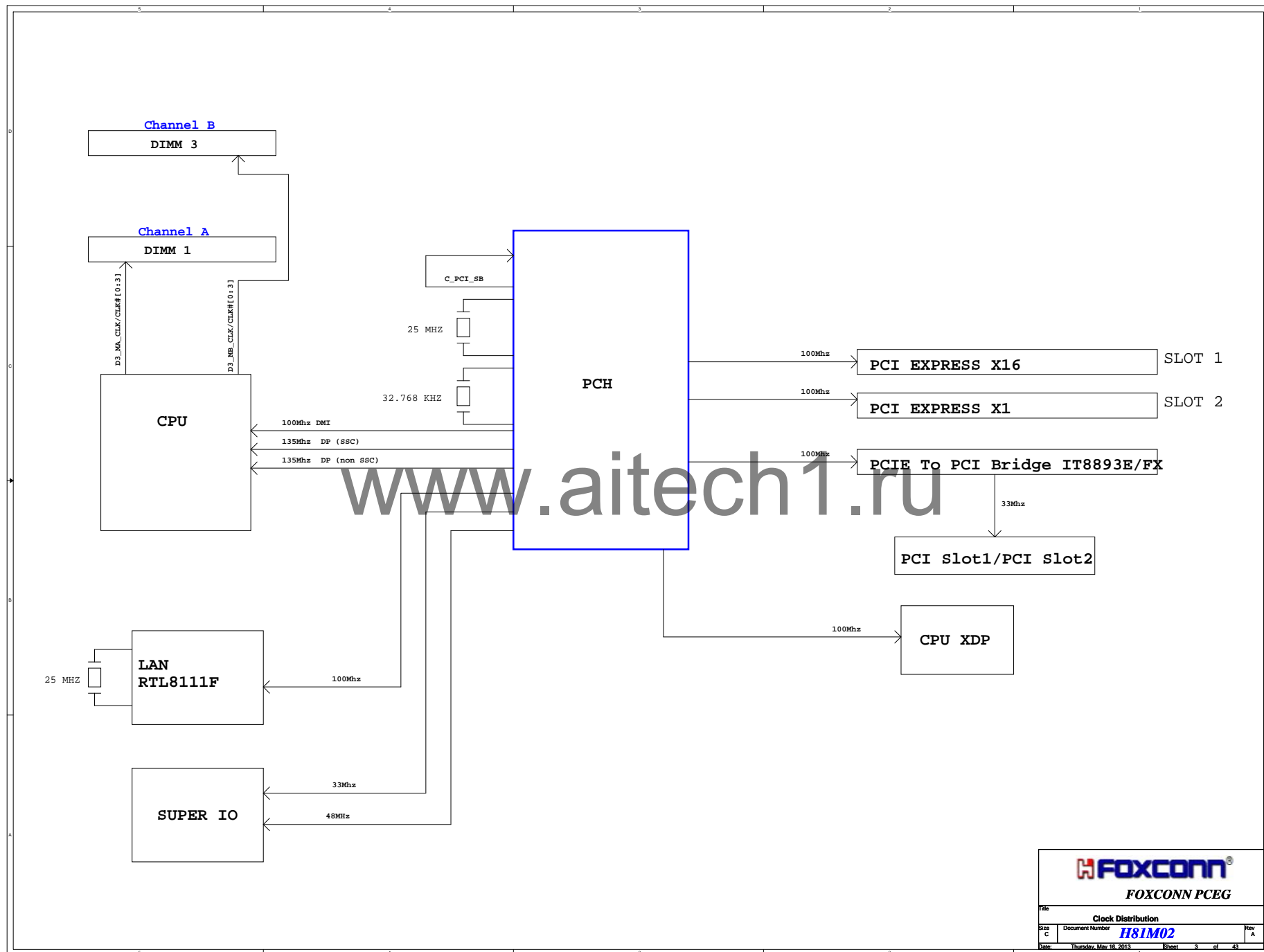
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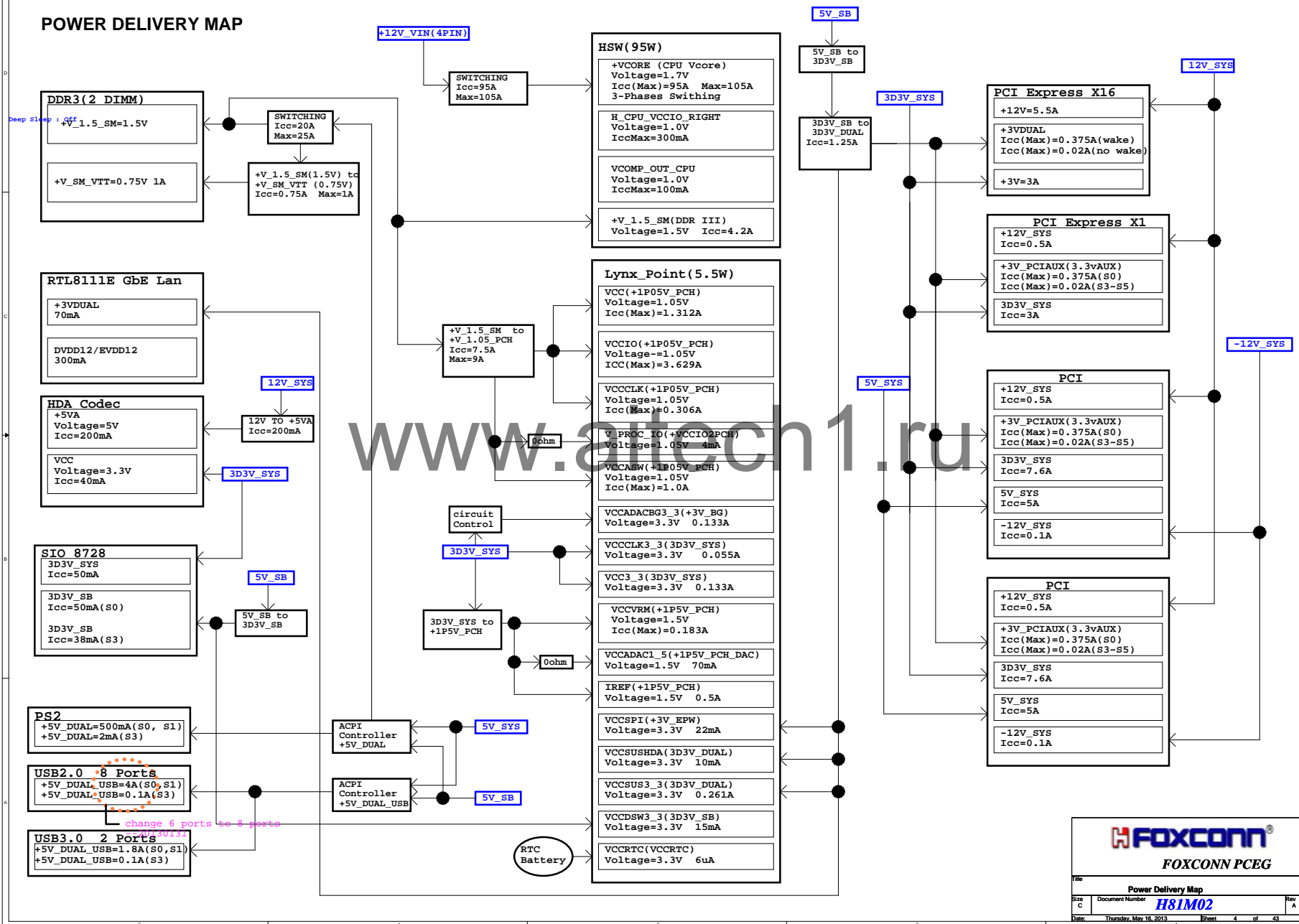
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SMBUS DIAGRAM



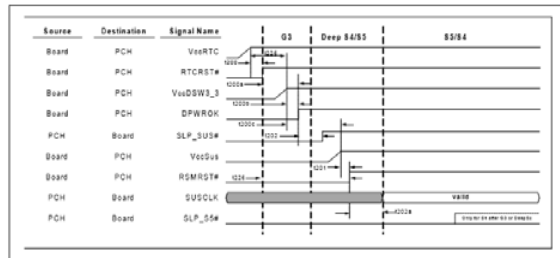


POWER DELIVERY MAP



Power Delivery Map		
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Figure 8-1. G3 w/RTC Loss to S4/S5 (With Deep Sx Support) Timing Diagram



Note: VCCSUS rail ramps up later in comparison to VCCDSW due to assumption that SLP_SUS# is used to control power to VCCSUS.

Figure 8-2. G3 w/RTC Loss to S4/S5 (Without Deep Sx Support) Timing Diagram

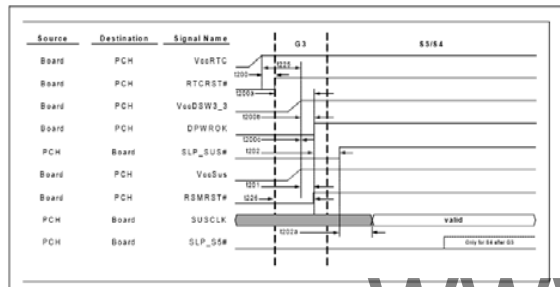
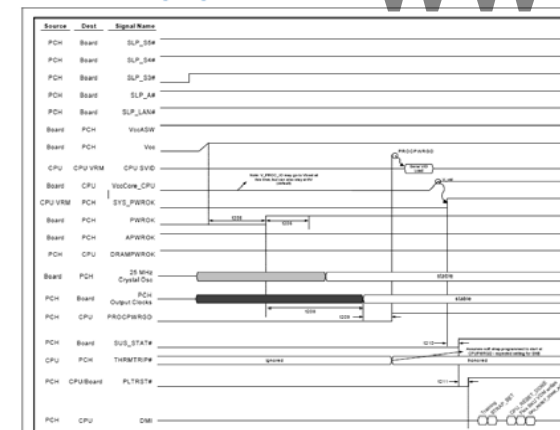
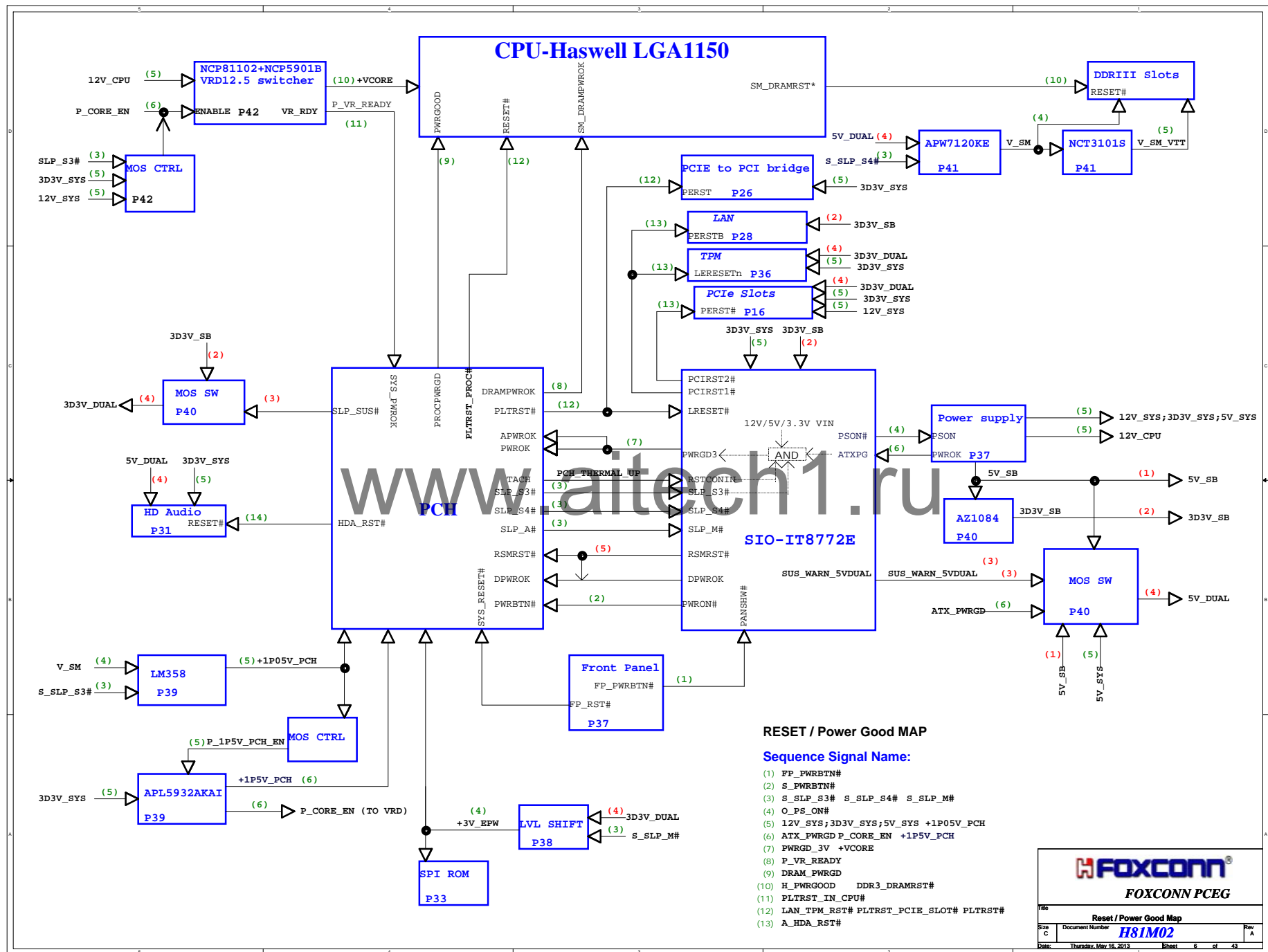


Figure 8-4. S3/M3 to S0 Timing Diagram





STRAPPING Table

CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal Default 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default

Strapping Options Peak

Option	Strapping Options	Notes
0	0	Reset CPU to UEFI
1	1	Reset CPU to BIOS
2	2	Reset CPU to UEFI

Table 34-6. PCH Digital Display Strapping Signals

Checklist Item	Recommendations	Direction	Comments
DDPC_CTRLDATA	Straps for digital port B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2K W resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2K W resistor. This signal should always be routed longer than DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2K W resistor and a Schottky diode. This signal should always be routed longer than DDPC_CTRLCLK by an inch. Also ensure schottky diode is not shared with DDPC_CTRLCLK.	BI	

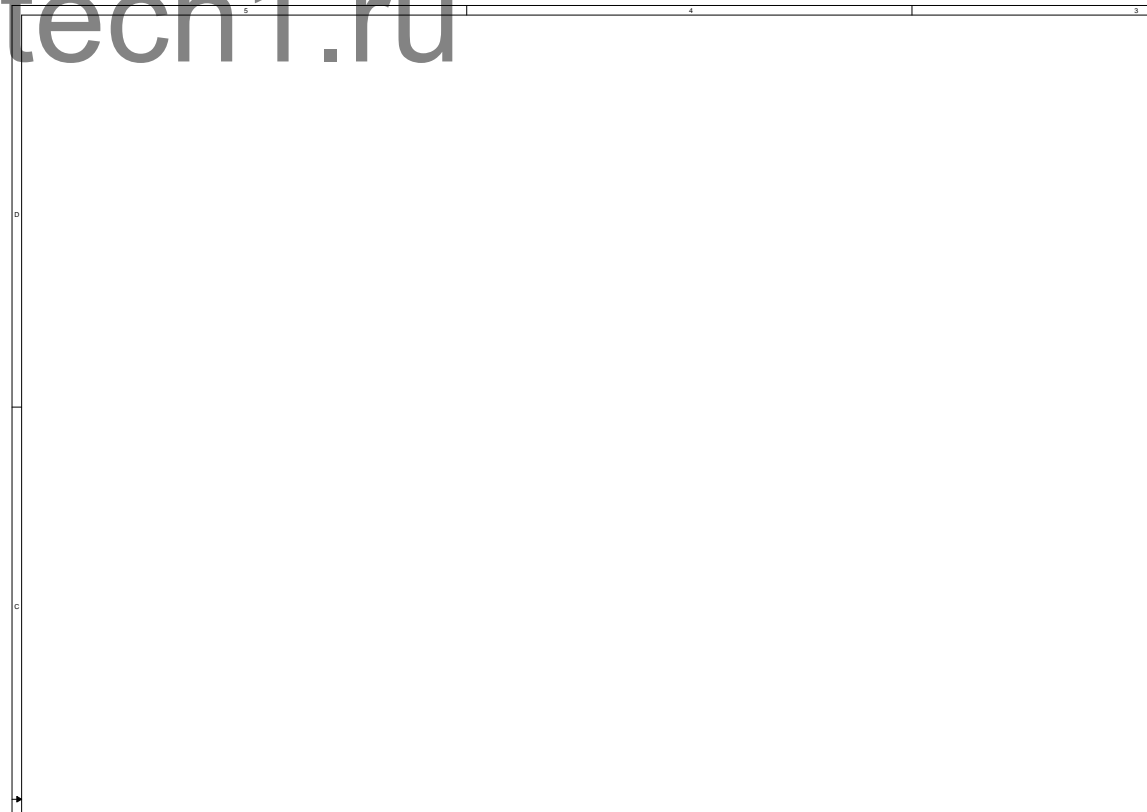
Table 36-18. Strapping Signals (Sheet 1 of 2)

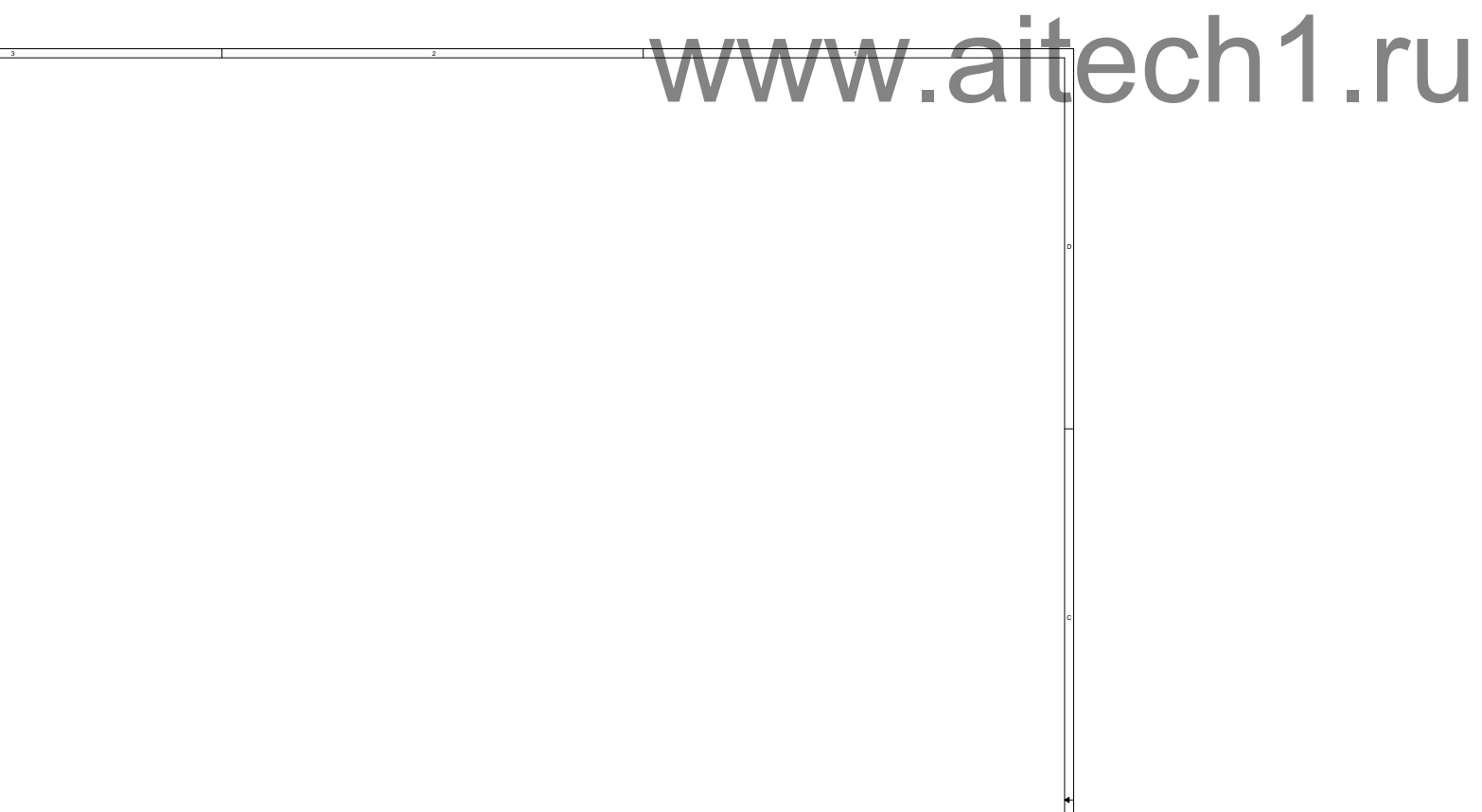
Name	Type	Recommendations	Reason/Impact
SPKR	I	Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2K-10K Ohm weak pull-up resistor.	
INIT3_3V#	I	Do not pull low.	
GPI055	I/O	Default Mode: Internal pull-up. Top Block Swap Mode: Connect to ground with 4.7K Ohm weak pull-down resistor.	
SATA1GP/ GPI019/ GPI051	I/O	Default (SPI) Left both SATA1GP/GPI019 and GPI051 floating. No pull up required. Boot from PCI Connect SATA1GP/GPI019 to ground with 1k Ohm pull-down resistor. Leave GPI051 Floating. Boot from LPC Connect both SATA1GP/GPI019 and GPI051 to ground with 1k Ohm pull-down resistor.	If LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Select will not affect SPI access initiated by Management Engine or Integrated GBE LAN. BI strap for server platform only.
GPI053	I/O	Do not pull low. Connect to ground with 1k Ohm pull-down resistor.	
HDA_SDO	I/O	Default Do not pull high. Disable ME in Manufacturing Mode Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.	Flash descriptor Override
SPI_MOSI	I/O	Internal weak pull down.Do not pull high.	DMI RX Termination Voltage
SAAT3GP/ GPI037	I/O	Enable TLS: Pull up with 1k Ohm to VccSus3.3. Default (Disable TLS): Leave NC. Internal pull down.	TLS confidentiality
GPI08	I/O	Internal weak pull up.Do not pull low.	

Table 36-18. Strapping Signals (Sheet 2 of 2)


Name	Type	Recommendations	Reason/Impact
GPI062/ SUSCLK	I/O	Internal weak pull up. Do not pull low.	On die PLL voltage regulator
GPI036	I/O	Internal weak pull down. Do not pull high.	
DDPB_CTRL_DATA DDPC_CTRL_DATA DDPD_CTRL_DATA	I/O	Straps for digital ports B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2K ohms resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2K ohms resistor. This signal should always be routed longer than DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage to the display connector. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2K ohms resistor. This signal should always be routed longer than SDVO/DDPC_CTRLCLK by an inch.	

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Title

GPIO Table

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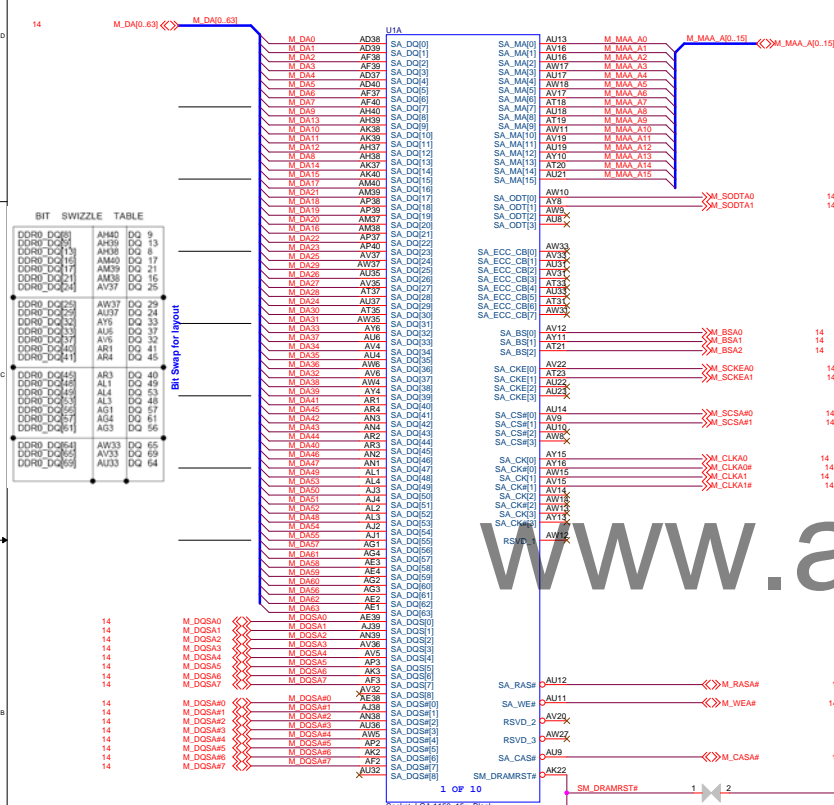
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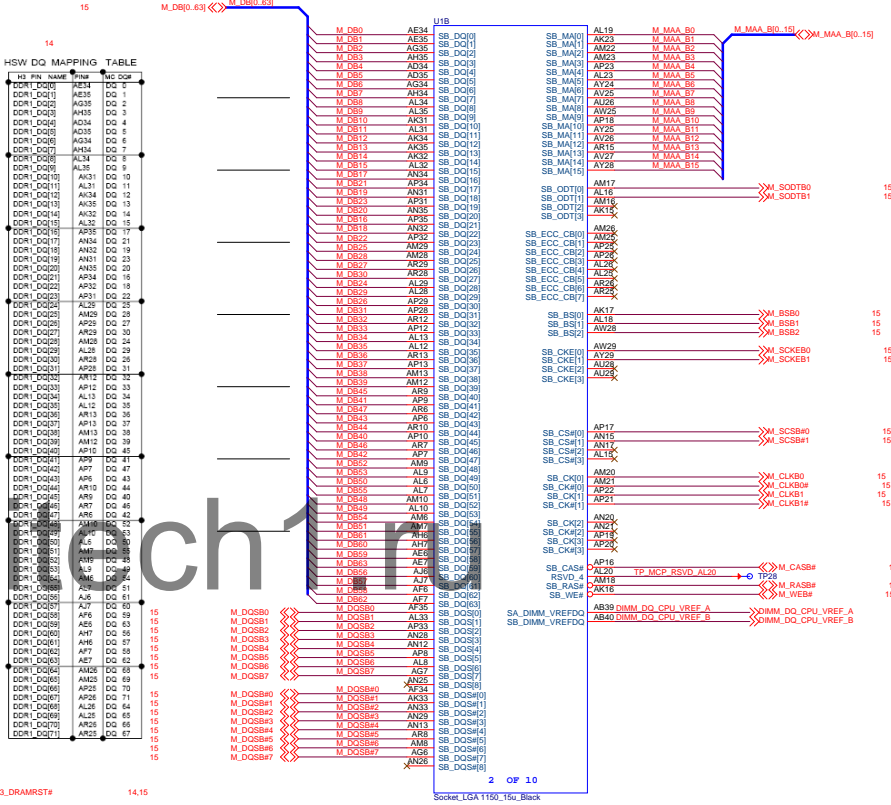
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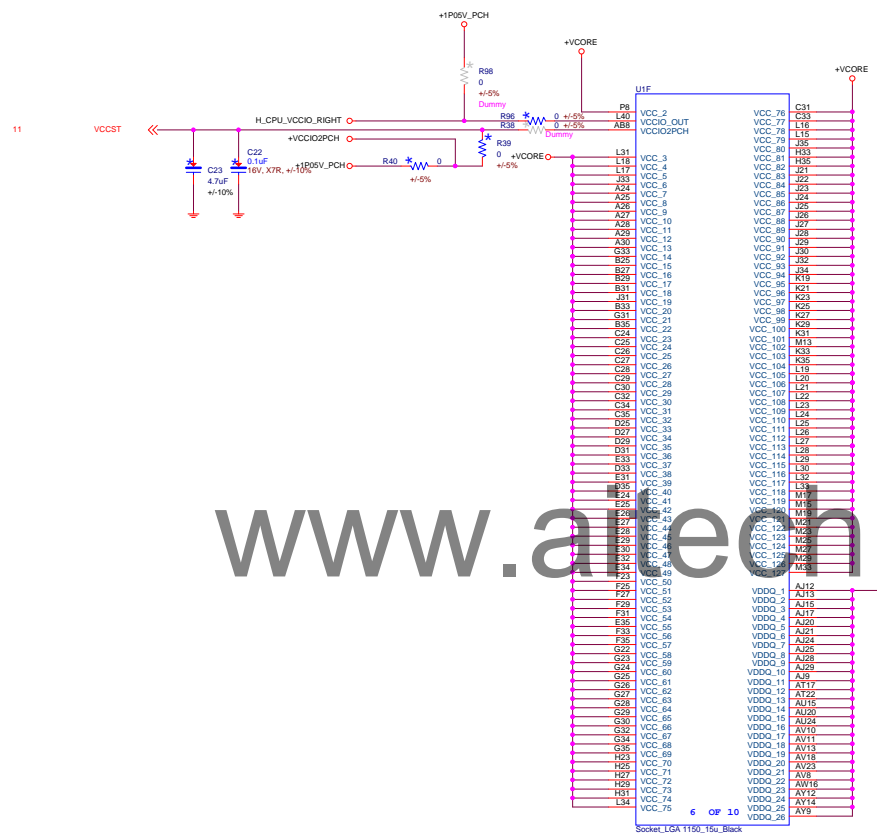
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DDR3 CH-A

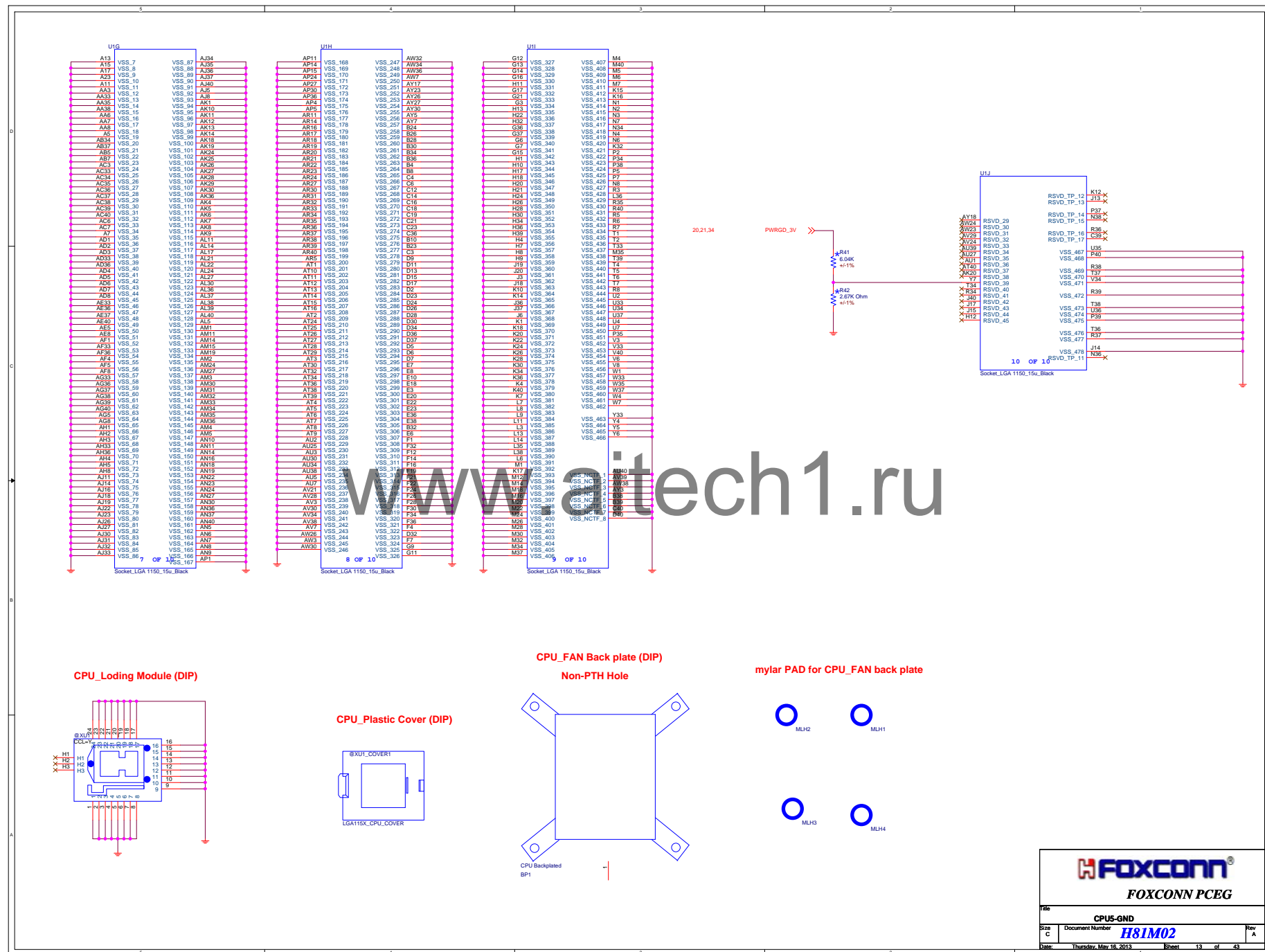


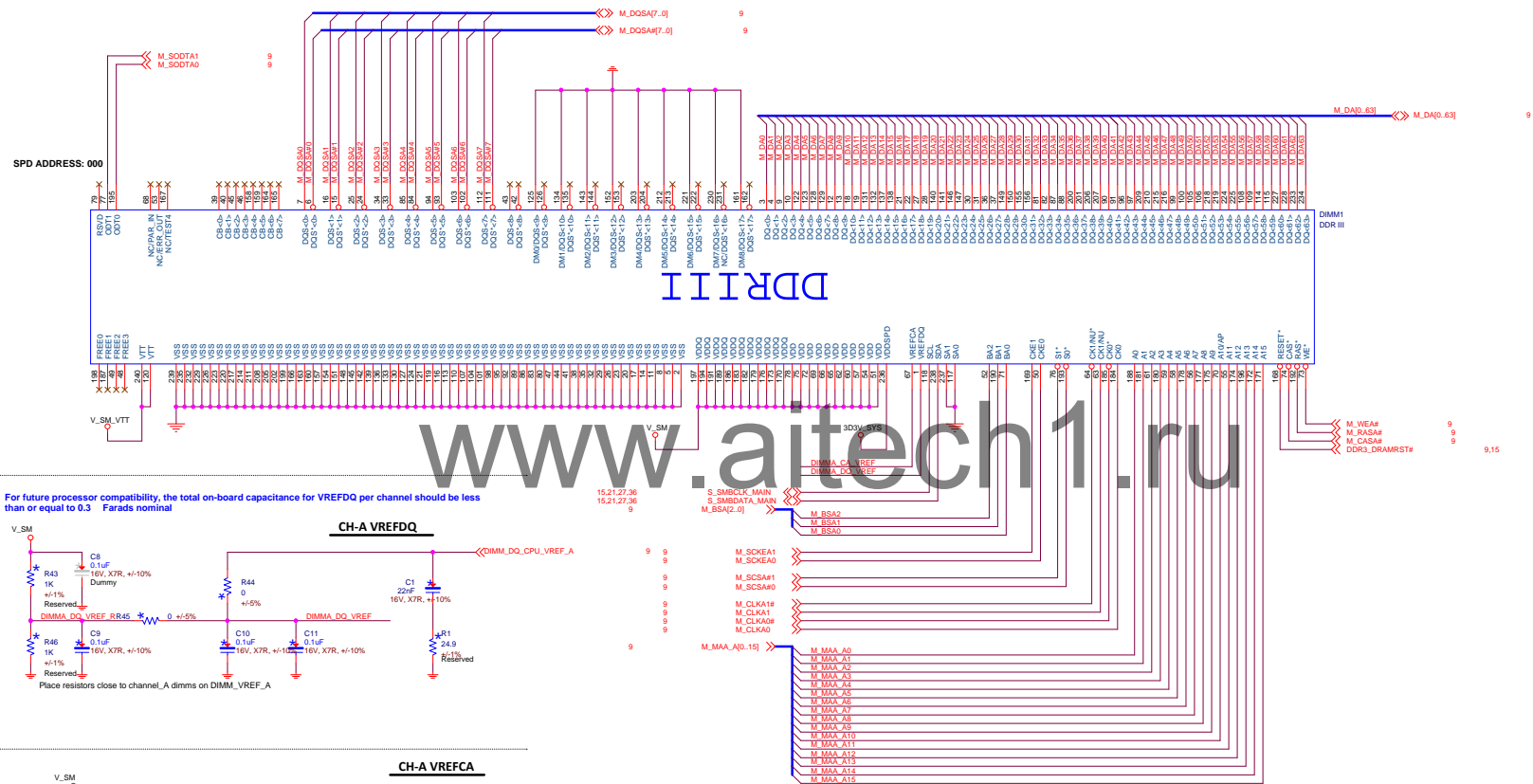
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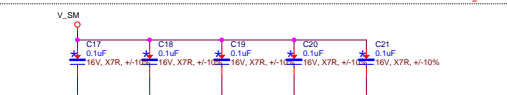
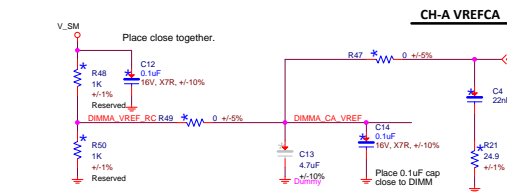
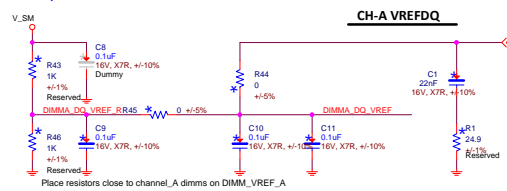


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For future processor compatibility, the total on-board capacitance for VREFDQ per channel should be less than or equal to 0.3 Farads nominal

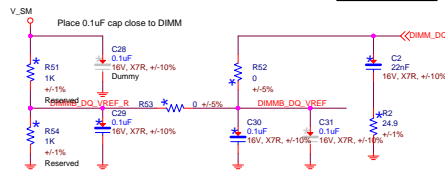


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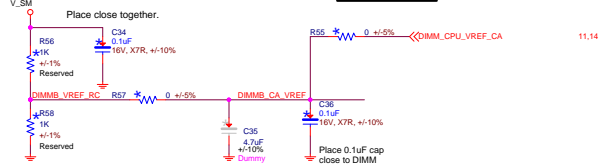
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CH-B VREFDQ



CH-B VREFCA

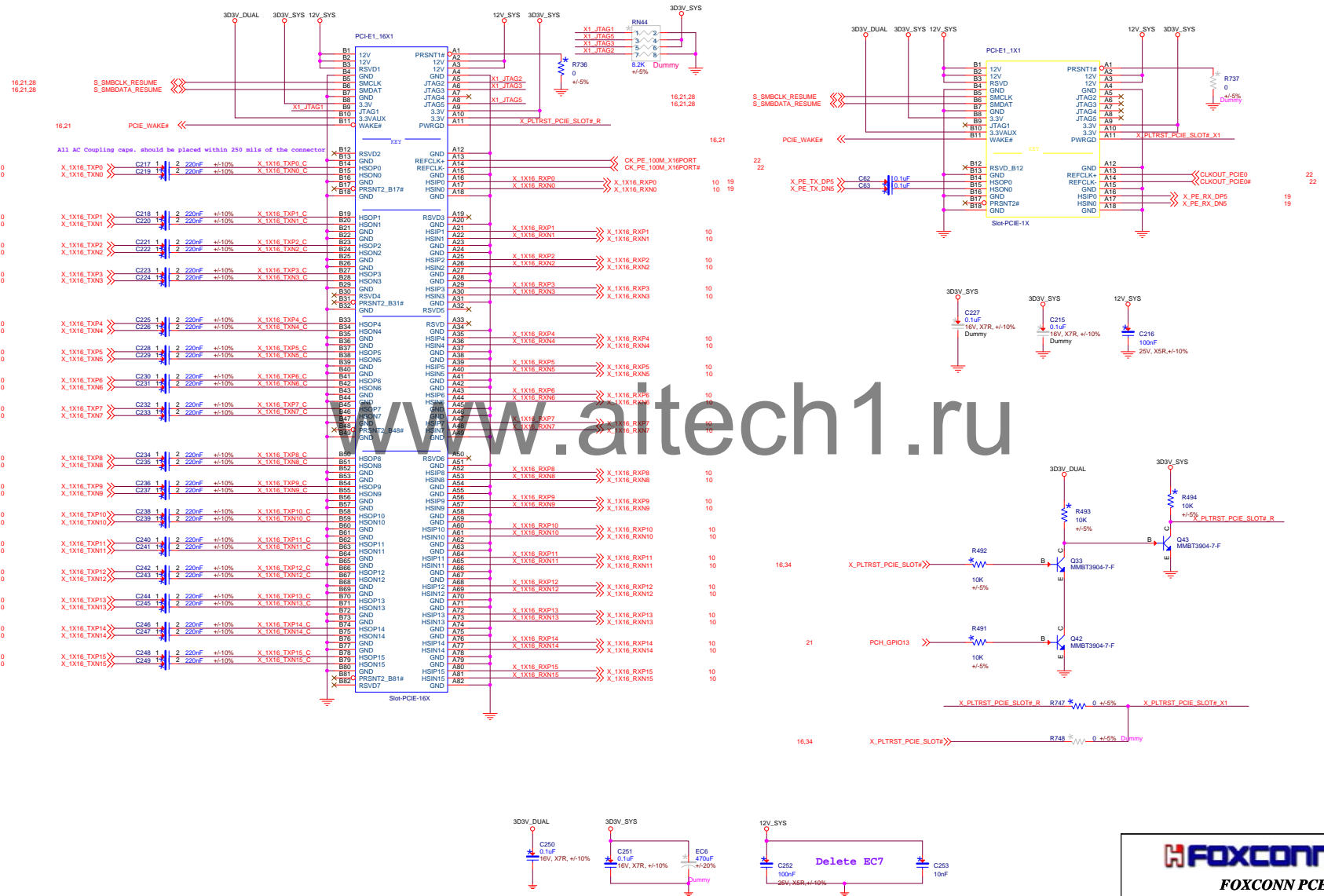


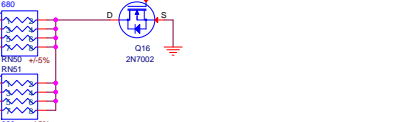
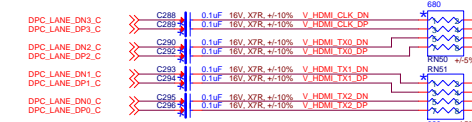
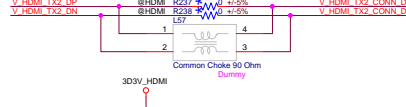
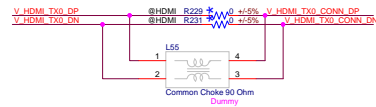
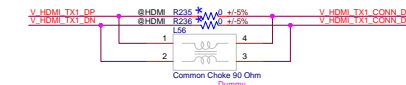
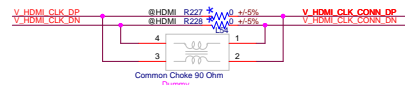
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PCI EXPRESS X1 SLOT1

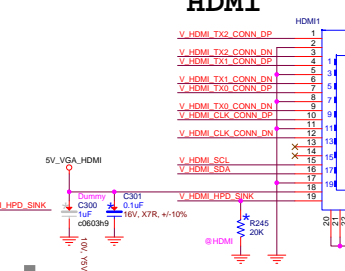
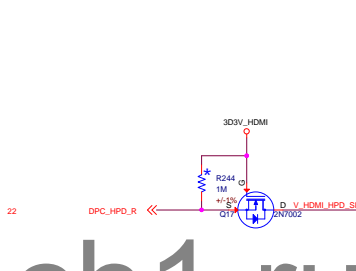
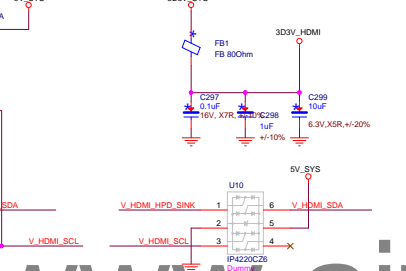
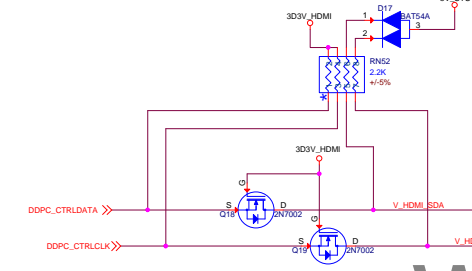
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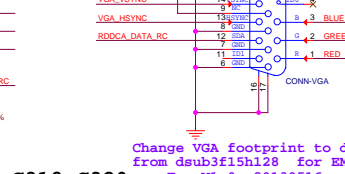
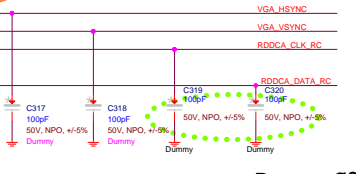
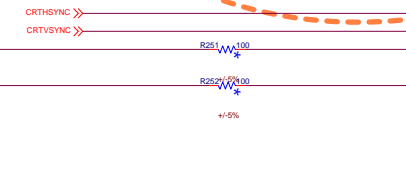
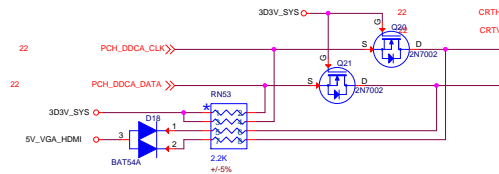
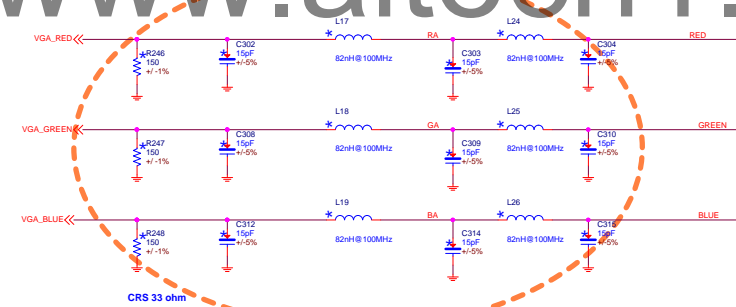
Delete DVI-D1,C287,R243,C291,L58 to L61
Delete colay resistors
(R230,R232,R233,R234,
R239,R240,R241,R242)
--20130218

Change HDMI to
(34043MP00-VPN-G) in BOM.



VGA

Change C302, C308, C312, C303,
C309, C314 to 15pF from 4.7pF.
Change L17, L18, L19 to 82nH from 27nH.
Reserved C304, C310, C315 15pF.
Delete R291, R350, R450 0ohm.
Add L24, L25, L26 82nH For EMI.
--For V1.0 20130509



Dummy C319,C320
--20130315

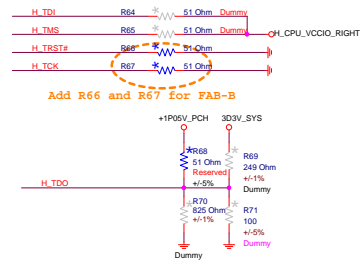
Add D19(Dummy),
R755 for TF
--For V1.0 20130504

Change VGA footprint to dsub3f15_4h128
from dsub3f15h128 for EMI
----For V1.0 20130516

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Intel CPU XDP Debug Connector



Add R66 and R67 for FAB-B

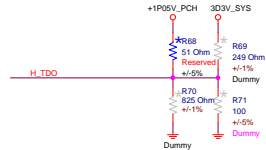
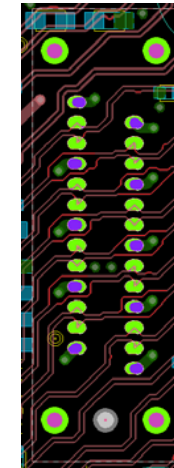


Table 3-1. Processor XDP Connector Pinout

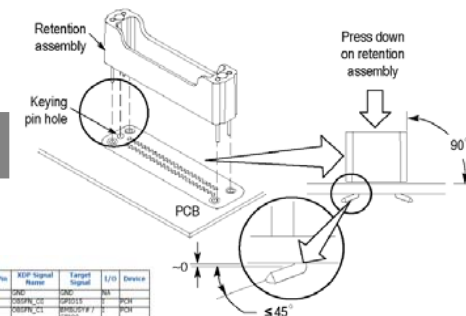
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Intel DMI LAI Footprint

This is footprint only . BOM is Dummy



Change for FAB-E



Intel PCH XDP Debug Connector

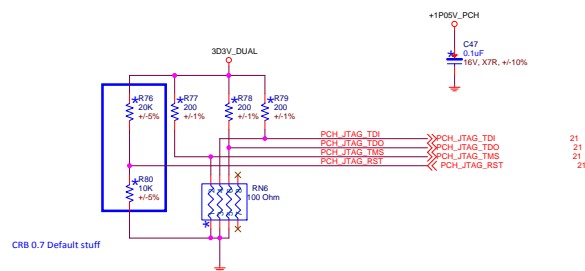


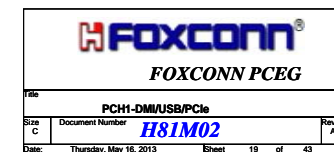
Table 4-1. PCH XDP Connector Pinout

No	XDP Signal Name	Target Signal	I/O	Device	No	XDP Signal Name	Target Signal	I/O	Device
1	OSRNG_A0	OSRNG	MS	4	OSRNG_C0	OSRNG	OSRNG	MS	4
2	OSRNG_A1	OSRNG	MS	4	OSRNG_C1	OSRNG	OSRNG	MS	4
3	OSRNG_A2	OSRNG	MS	4	OSRNG_C2	OSRNG	OSRNG	MS	4
4	OSRNG_A3	OSRNG	MS	4	OSRNG_C3	OSRNG	OSRNG	MS	4
5	OSRNG_A4	OSRNG	MS	4	OSRNG_C4	OSRNG	OSRNG	MS	4
6	OSRNG_A5	OSRNG	MS	4	OSRNG_C5	OSRNG	OSRNG	MS	4
7	OSRNG_A6	OSRNG	MS	4	OSRNG_C6	OSRNG	OSRNG	MS	4
8	OSRNG_A7	OSRNG	MS	4	OSRNG_C7	OSRNG	OSRNG	MS	4
9	OSRNG_A8	OSRNG	MS	4	OSRNG_C8	OSRNG	OSRNG	MS	4
10	OSRNG_A9	OSRNG	MS	4	OSRNG_C9	OSRNG	OSRNG	MS	4
11	OSRNG_A10	OSRNG	MS	4	OSRNG_C10	OSRNG	OSRNG	MS	4
12	OSRNG_A11	OSRNG	MS	4	OSRNG_C11	OSRNG	OSRNG	MS	4
13	OSRNG_A12	OSRNG	MS	4	OSRNG_C12	OSRNG	OSRNG	MS	4
14	OSRNG_A13	OSRNG	MS	4	OSRNG_C13	OSRNG	OSRNG	MS	4
15	OSRNG_A14	OSRNG	MS	4	OSRNG_C14	OSRNG	OSRNG	MS	4
16	OSRNG_A15	OSRNG	MS	4	OSRNG_C15	OSRNG	OSRNG	MS	4
17	OSRNG_A16	OSRNG	MS	4	OSRNG_C16	OSRNG	OSRNG	MS	4
18	OSRNG_A17	OSRNG	MS	4	OSRNG_C17	OSRNG	OSRNG	MS	4
19	OSRNG_A18	OSRNG	MS	4	OSRNG_C18	OSRNG	OSRNG	MS	4
20	OSRNG_A19	OSRNG	MS	4	OSRNG_C19	OSRNG	OSRNG	MS	4
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26	OSRNG_A25	OSRNG	MS	4	OSRNG_C25	OSRNG	OSRNG	MS	4
27	OSRNG_A26	OSRNG	MS	4	OSRNG_C26	OSRNG	OSRNG	MS	4
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46	OSRNG_A45	OSRNG	MS	4	OSRNG_C45	OSRNG	OSRNG	MS	4
47	OSRNG_A46	OSRNG	MS	4	OSRNG_C46	OSRNG	OSRNG	MS	4
48	OSRNG_A47	OSRNG	MS	4	OSRNG_C47	OSRNG	OSRNG	MS	4
49	OSRNG_A48	OSRNG	MS	4	OSRNG_C48	OSRNG	OSRNG	MS	4
50	OSRNG_A49	OSRNG	MS	4	OSRNG_C49	OSRNG	OSRNG	MS	4
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58	OSRNG_A57	OSRNG	MS	4	OSRNG_C57	OSRNG	OSRNG	MS	4
59	OSRNG_A58	OSRNG	MS	4	OSRNG_C58	OSRNG	OSRNG	MS	4
60	OSRNG_A59	OSRNG	MS	4	OSRNG_C59	OSRNG	OSRNG	MS	4
61	OSRNG_A60	OSRNG	MS	4	OSRNG_C60	OSRNG	OSRNG	MS	4
62	OSRNG_A61	OSRNG	MS	4	OSRNG_C61	OSRNG	OSRNG	MS	4
63	OSRNG_A62	OSRNG	MS	4	OSRNG_C62	OSRNG	OSRNG	MS	4
64	OSRNG_A63	OSRNG	MS	4	OSRNG_C63	OSRNG	OSRNG	MS	4
65	OSRNG_A64	OSRNG	MS	4	OSRNG_C64	OSRNG	OSRNG	MS	4
66	OSRNG_A65	OSRNG	MS	4	OSRNG_C65	OSRNG	OSRNG	MS	4
67	OSRNG_A66	OSRNG	MS	4	OSRNG_C66	OSRNG	OSRNG	MS	4
68	OSRNG_A67	OSRNG	MS	4	OSRNG_C67	OSRNG	OSRNG	MS	4
69	OSRNG_A68	OSRNG	MS	4	OSRNG_C68	OSRNG	OSRNG	MS	4
70	OSRNG_A69	OSRNG	MS	4	OSRNG_C69	OSRNG	OSRNG	MS	4
71	OSRNG_A70	OSRNG	MS	4	OSRNG_C70	OSRNG	OSRNG	MS	4
72	OSRNG_A71	OSRNG	MS	4	OSRNG_C71	OSRNG	OSRNG	MS	4
73	OSRNG_A72	OSRNG	MS	4	OSRNG_C72	OSRNG	OSRNG	MS	4
74	OSRNG_A73	OSRNG	MS	4	OSRNG_C73	OSRNG	OSRNG	MS	4
75	OSRNG_A74	OSRNG	MS	4	OSRNG_C74	OSRNG	OSRNG	MS	4
76	OSRNG_A75	OSRNG	MS	4	OSRNG_C75	OSRNG	OSRNG	MS	4
77	OSRNG_A76	OSRNG	MS	4	OSRNG_C76	OSRNG	OSRNG	MS	4
78	OSRNG_A77	OSRNG	MS	4	OSRNG_C77	OSRNG	OSRNG	MS	4
79	OSRNG_A78	OSRNG	MS	4	OSRNG_C78	OSRNG	OSRNG	MS	4
80	OSRNG_A79	OSRNG	MS	4	OSRNG_C79	OSRNG	OSRNG	MS	4
81	OSRNG_A80	OSRNG	MS	4	OSRNG_C80	OSRNG	OSRNG	MS	4
82	OSRNG_A81	OSRNG	MS	4	OSRNG_C81	OSRNG	OSRNG	MS	4
83	OSRNG_A82	OSRNG	MS	4	OSRNG_C82	OSRNG	OSRNG	MS	4
84	OSRNG_A83	OSRNG	MS	4	OSRNG_C83	OSRNG	OSRNG	MS	4
85	OSRNG_A84	OSRNG	MS	4	OSRNG_C84	OSRNG	OSRNG	MS	4
86	OSRNG_A85	OSRNG	MS	4	OSRNG_C85	OSRNG	OSRNG	MS	4
87	OSRNG_A86	OSRNG	MS	4	OSRNG_C86	OSRNG	OSRNG	MS	4
88	OSRNG_A87	OSRNG	MS	4	OSRNG_C87	OSRNG	OSRNG	MS	4
89	OSRNG_A88	OSRNG	MS	4	OSRNG_C88	OSRNG	OSRNG	MS	4
90	OSRNG_A89	OSRNG	MS	4	OSRNG_C89	OSRNG	OSRNG	MS	4
91	OSRNG_A90	OSRNG	MS	4	OSRNG_C90	OSRNG	OSRNG	MS	4
92	OSRNG_A91	OSRNG	MS	4	OSRNG_C91	OSRNG	OSRNG	MS	4
93	OSRNG_A92	OSRNG	MS	4	OSRNG_C92	OSRNG	OSRNG	MS	4
94	OSRNG_A93	OSRNG	MS	4	OSRNG_C93	OSRNG	OSRNG	MS	4
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96	OSRNG_A95	OSRNG	MS	4	OSRNG_C95	OSRNG	OSRNG	MS	4
97	OSRNG_A96	OSRNG	MS	4	OSRNG_C96	OSRNG	OSRNG	MS	4
98	OSRNG_A97	OSRNG	MS	4	OSRNG_C97	OSRNG	OSRNG	MS	4
99	OSRNG_A98	OSRNG	MS	4	OSRNG_C98	OSRNG	OSRNG	MS	4
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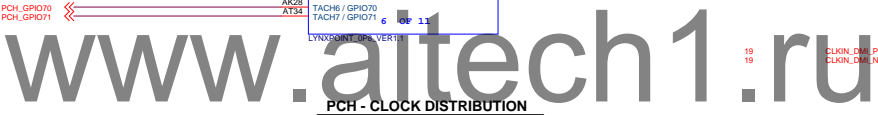
Change for FAB-B

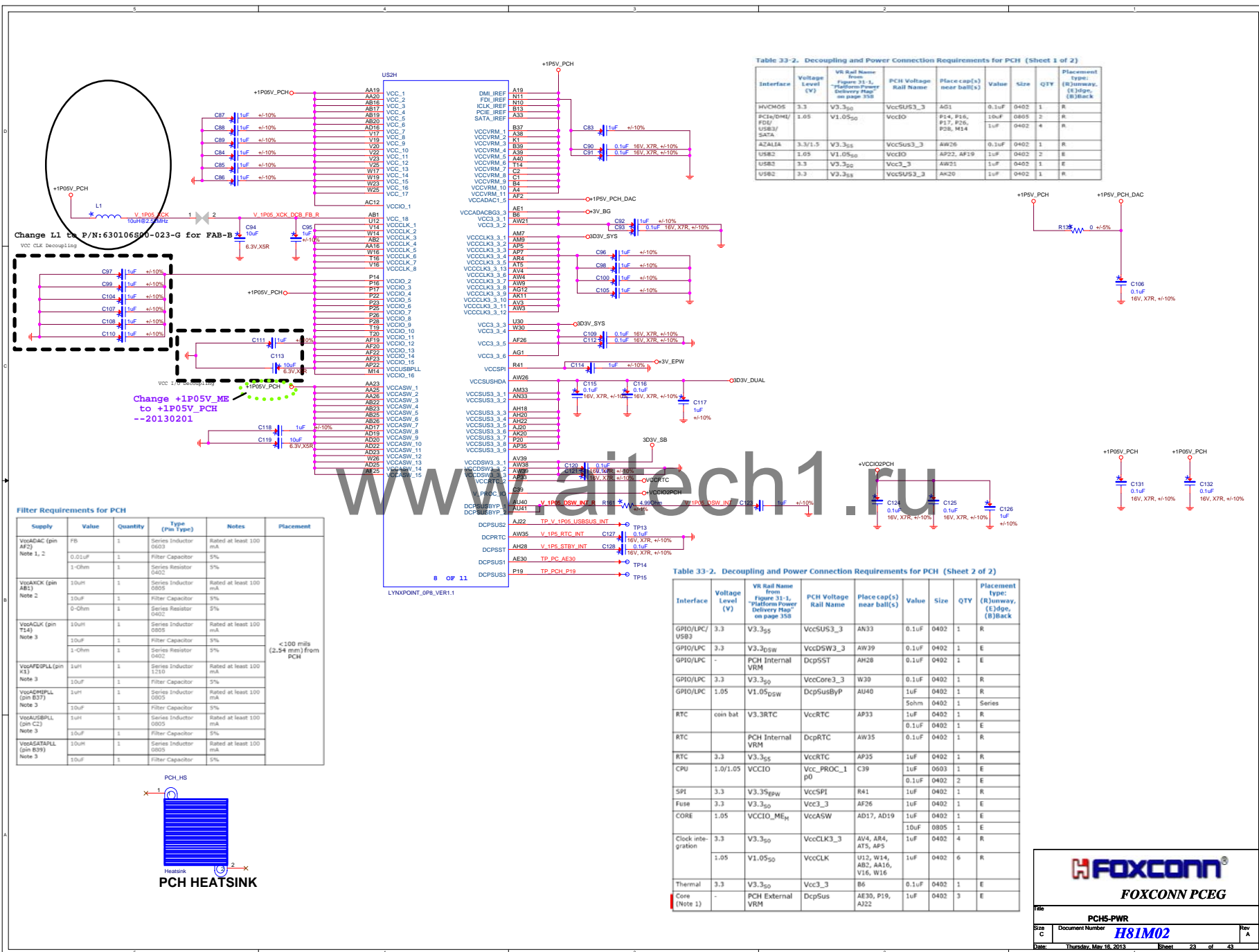
Change for FAB-B

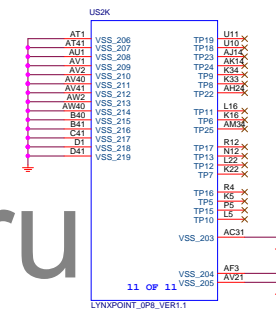
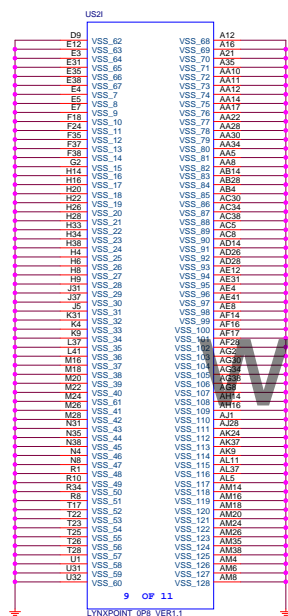






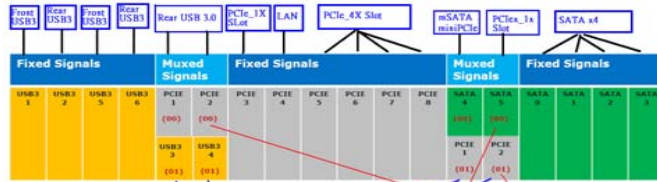




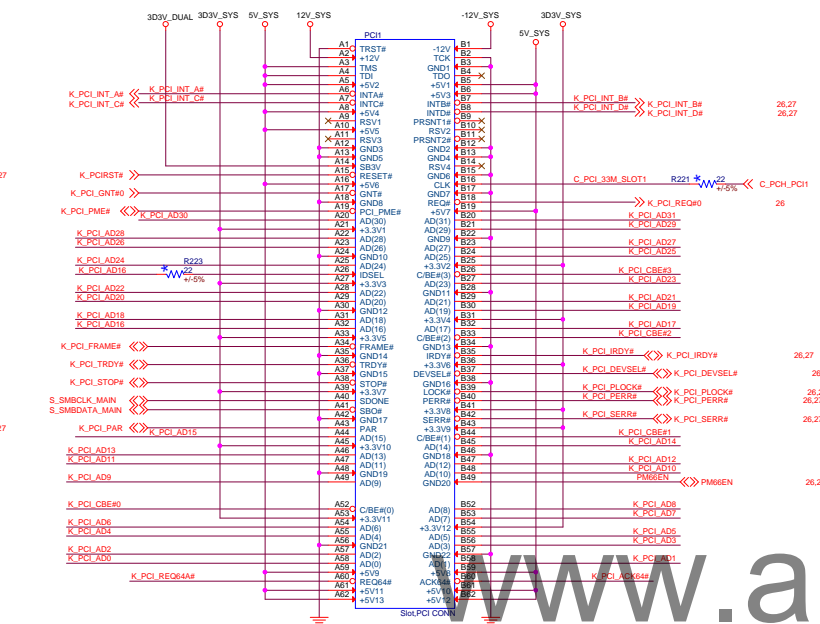


Lynx Point I/O Flexibility

- New architecture allows some I/O Ports to be configured at time of system design



PCI 1

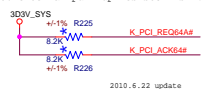


```

IRQ:  A B C D
IDSEL: AD16
REQ/GNT: 0

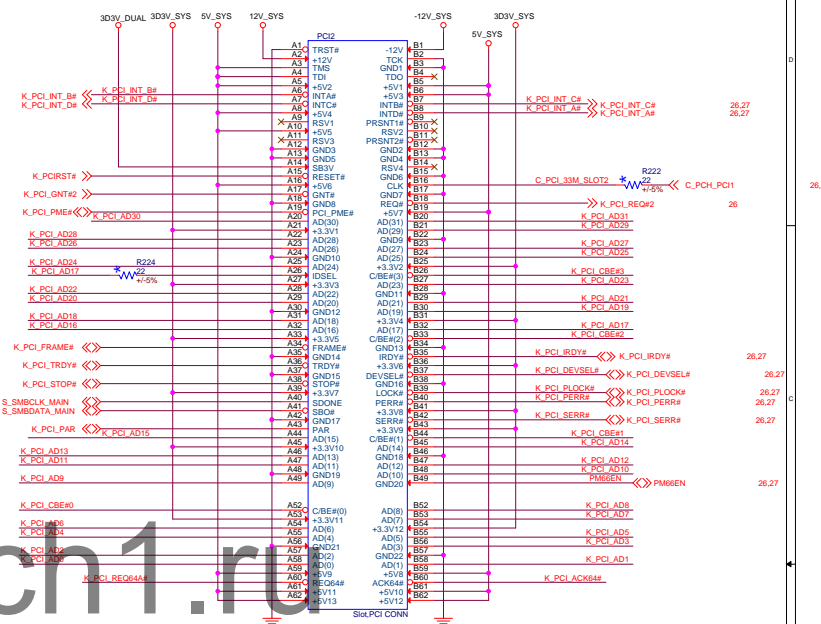
```

PCI BUS if use 5V external pull up resistor is 2.7K



2010.6.22 update

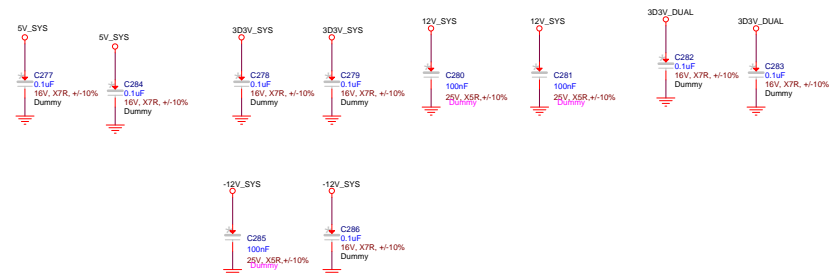
PCI 2



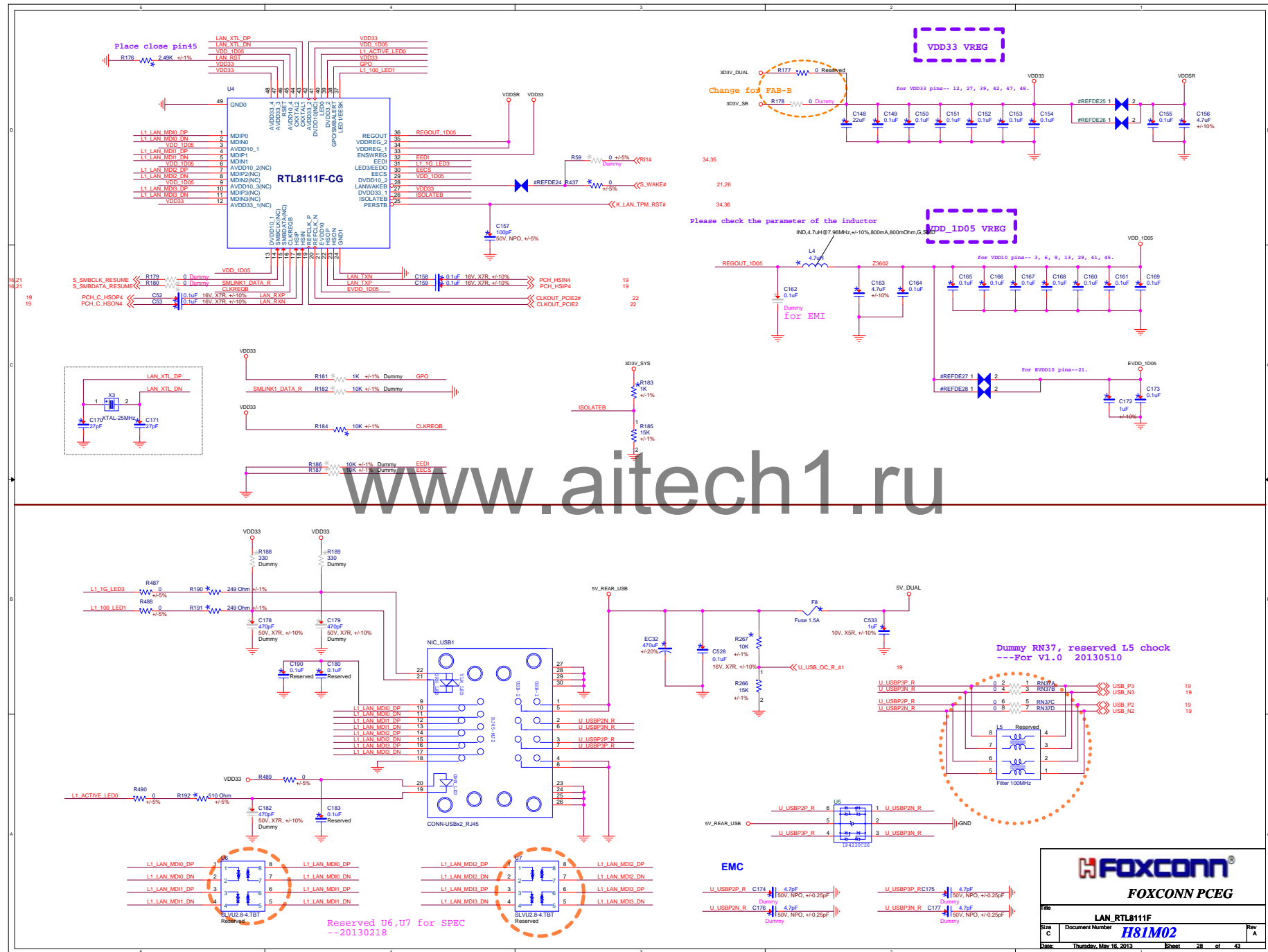
```

IRQ: B C D A
IDSEL: AD17
REQ/GNT: 2

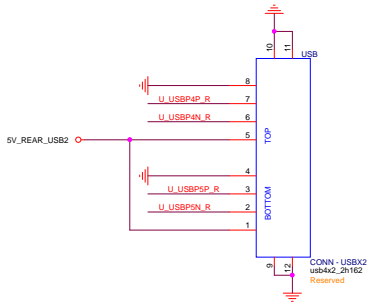
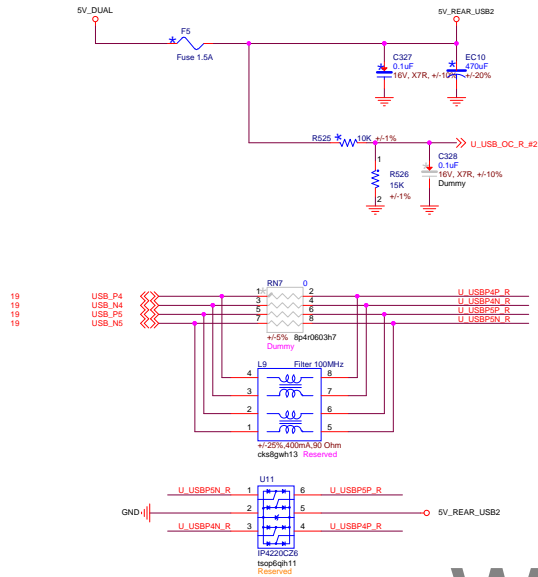
```



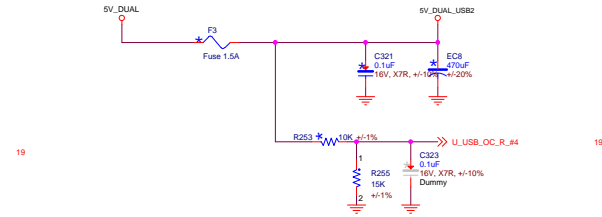
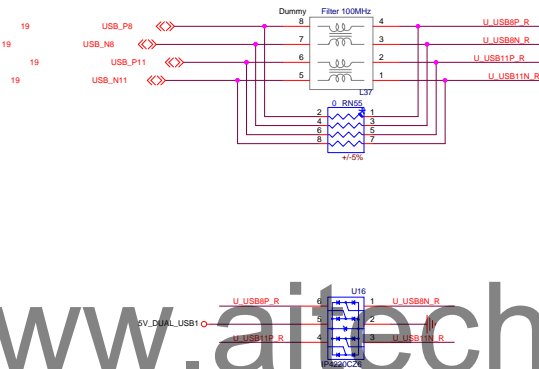
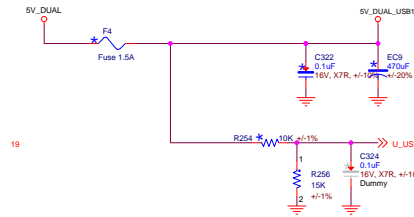
Title			
PCI SLOT X2			
Size	Document Number	Rev	
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Date:	Thursday, May 16, 2013	Sheet	27 of 43



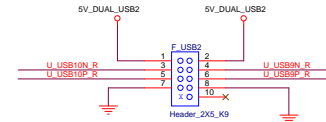
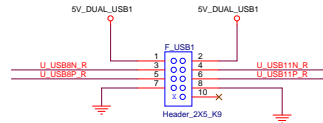
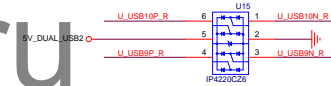
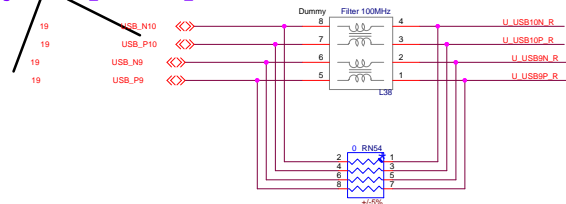
Front_USB1



Front_USB2

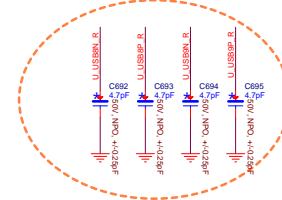
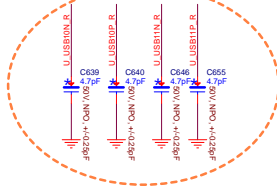


Change NET:USB_8 and USB_11
Change NET:USB_10 and USB_11



From Dummy to Reserved with EMC require for FAB-B

From Dummy to Reserved with EMC require for FAB-B

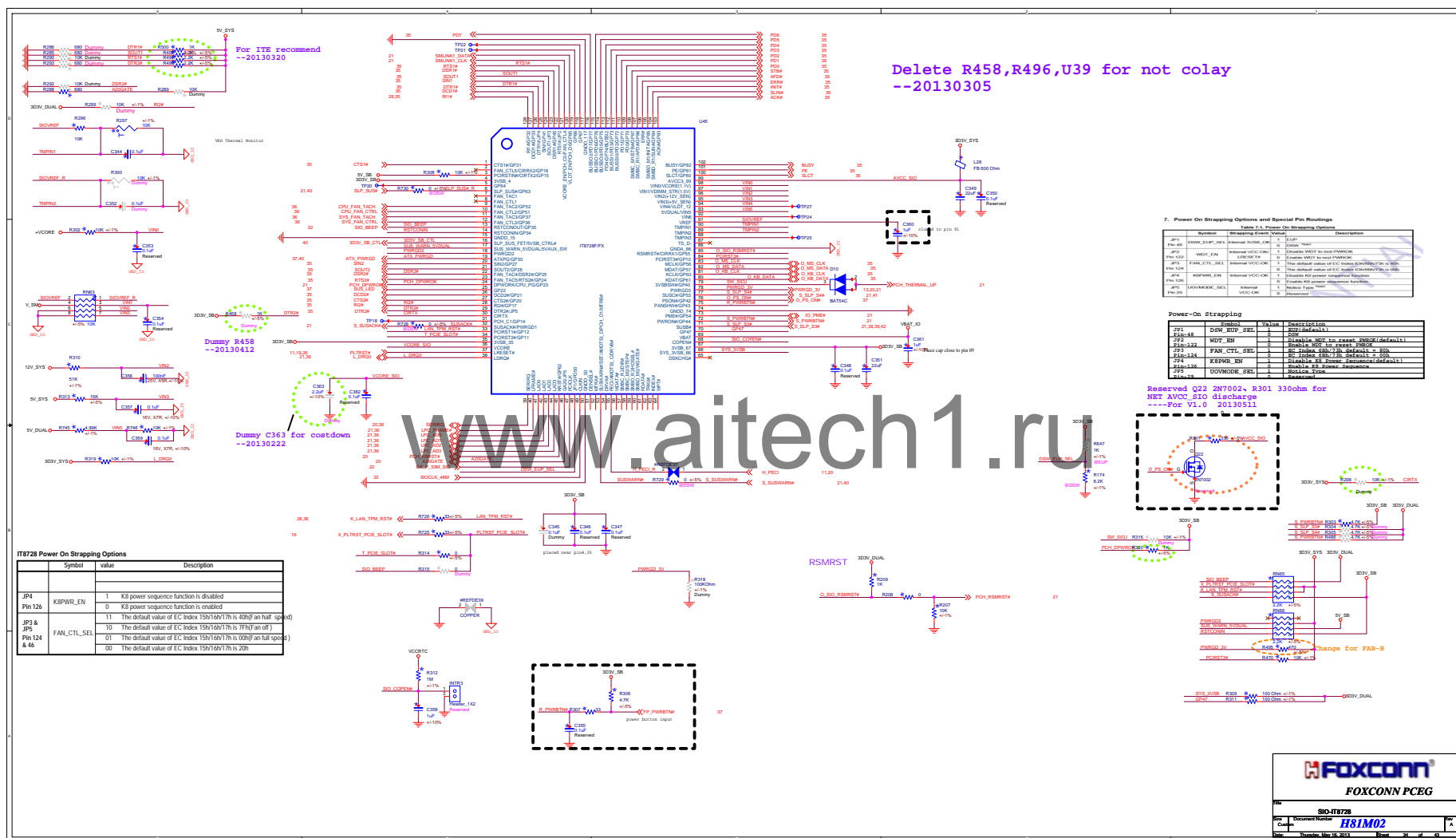
**FOXCONN PCEG**

File			
USB 2.0			
Size C	Document Number	<i>H81M02</i>	Rev A
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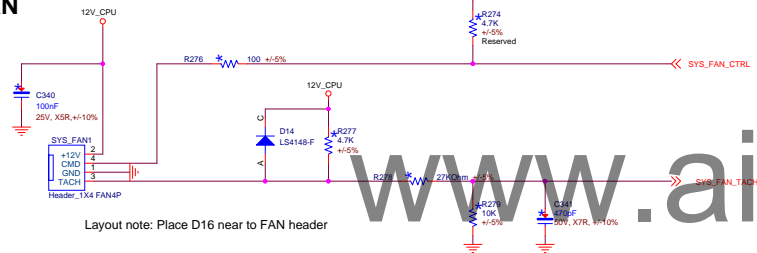
SPI SOCKET Primary

Place close to SPI ROM

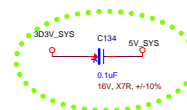
21
21



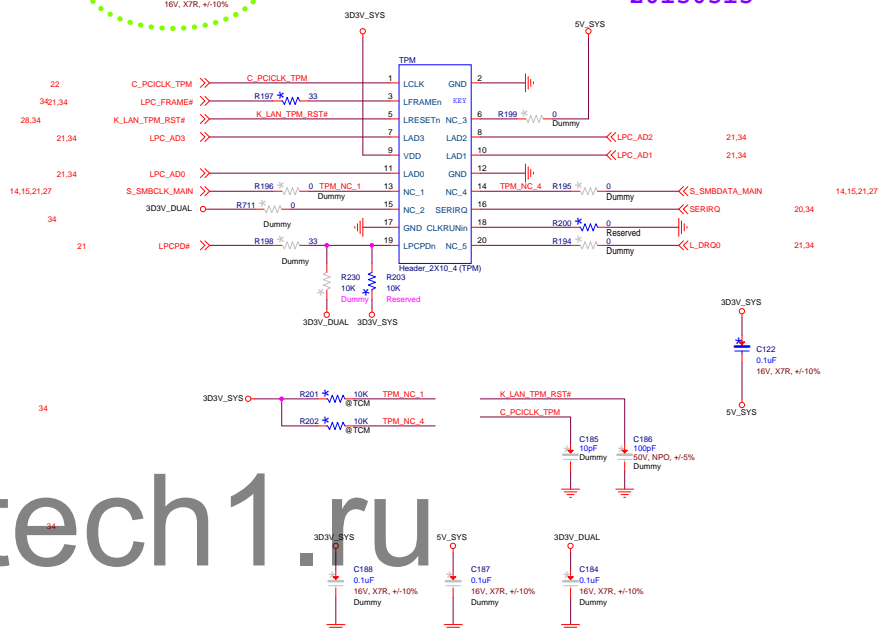
Change FAN Power from 12V_SYS to 12V_CPU
--20130301



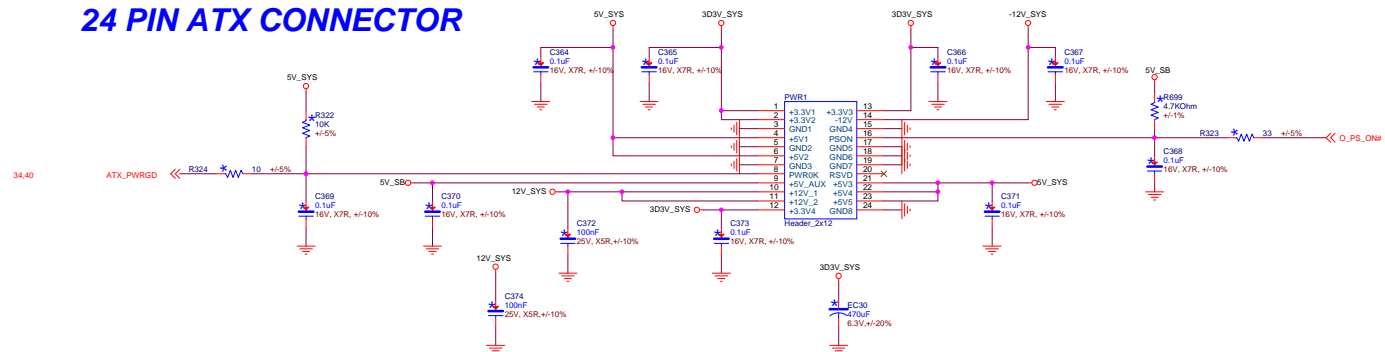
TPM



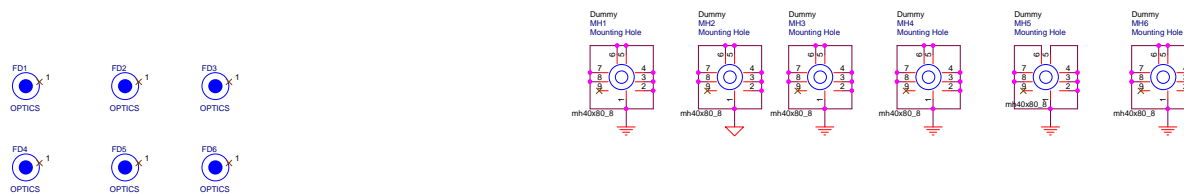
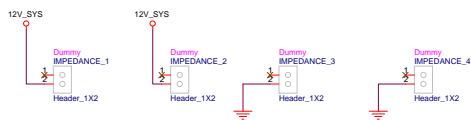
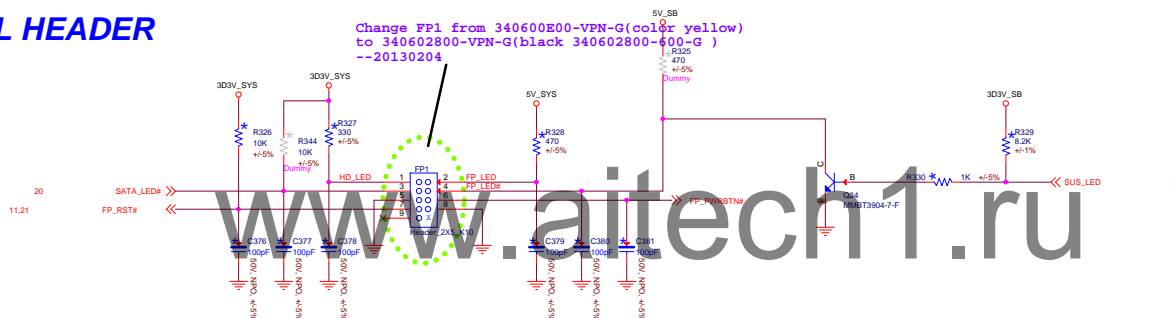
```
Dummy R199,R711
Reserved R200,R203
--20130313
```

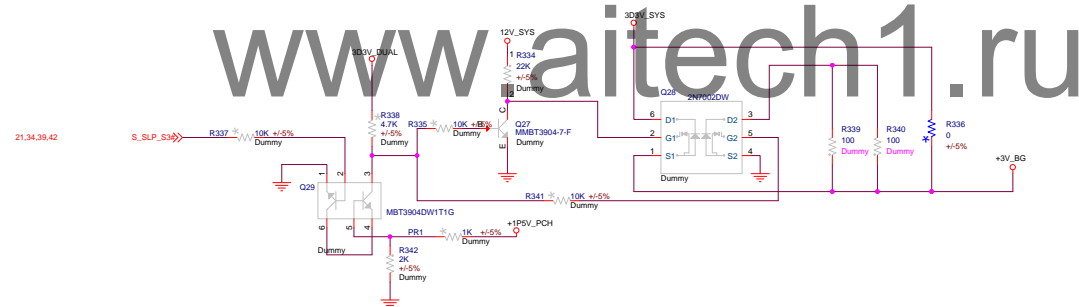


24 PIN ATX CONNECTOR

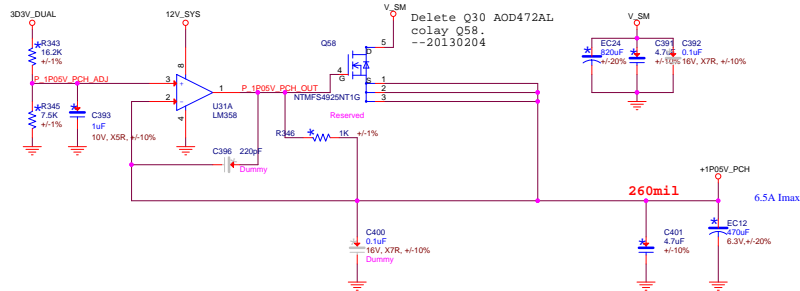


FRONT PANEL HEADER

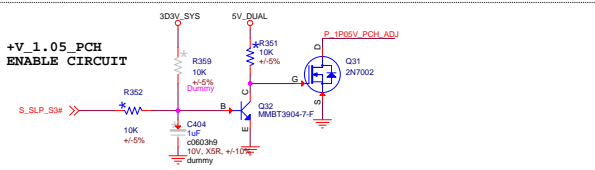




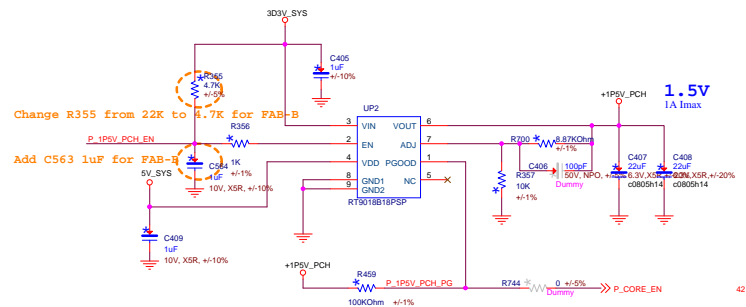
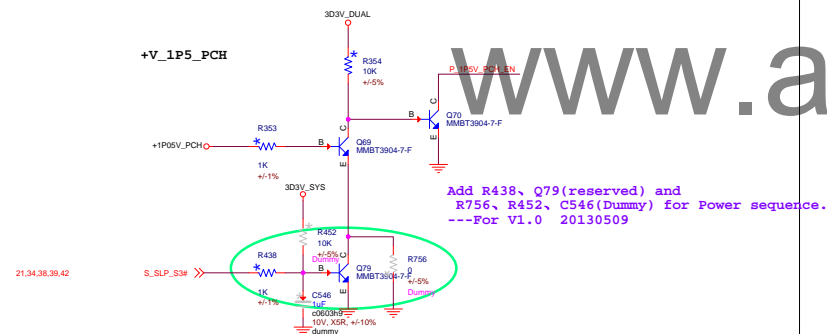
+V_1.05_PCH



+V_1.05_PCH ENABLE CIRCUIT



+V_1P5_PCH



+V_1.05_ME

www.aitech1.ru

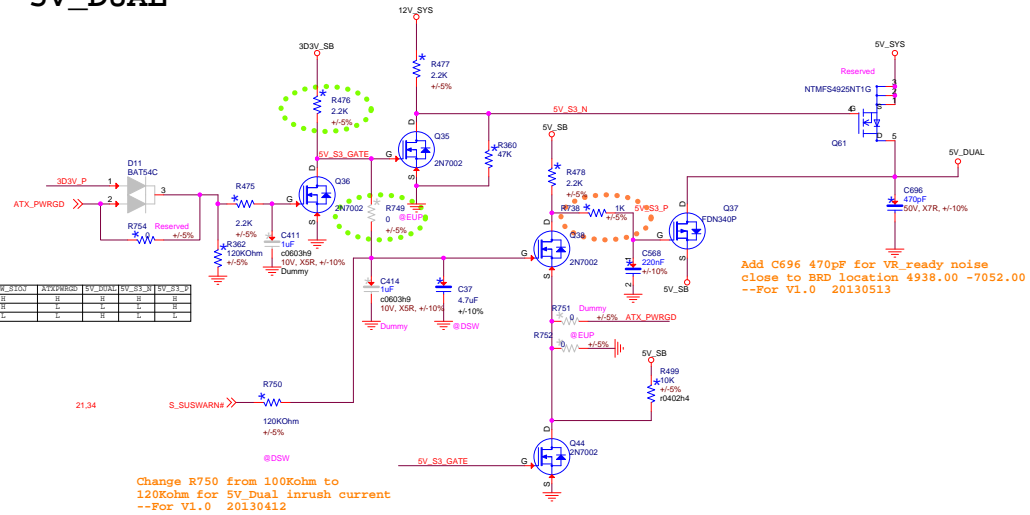


FOXCONN PCEG

File	1.05V_PCH	Rev
Size	Document Number	H81M02
C	Date	Thursday, May 16, 2013

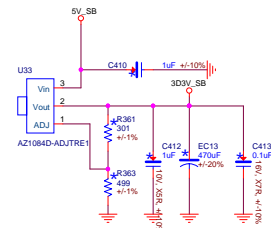
Sheet 39 of 43

5V_DUAL



3D3V_SB

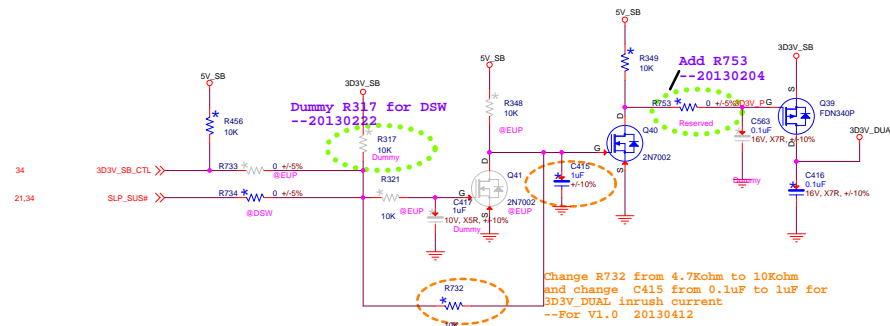
Max. output current = 3A



Vout=Vref(1+R2/R1)+IadjR2
R1 is Up Resistor.
Iadj=50uA
Vref=1.25V

www.aitech1.ru

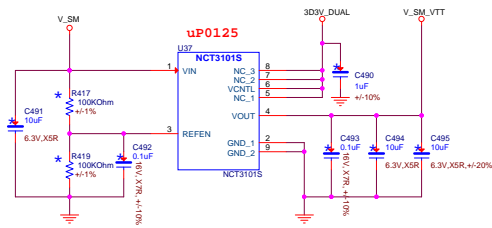
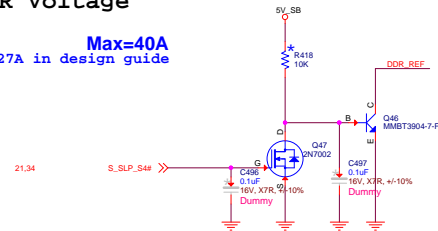
3D3V_DUAL



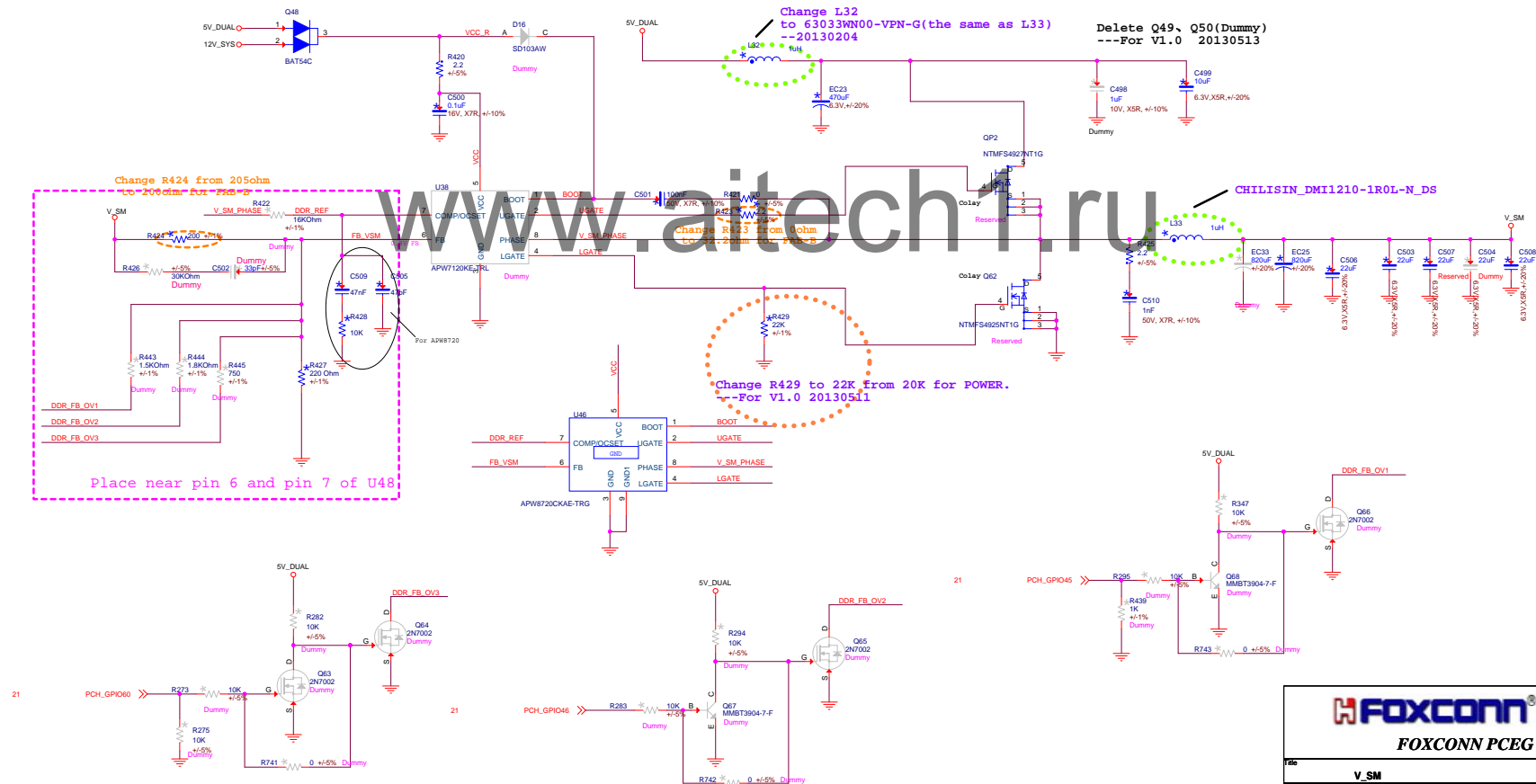
FOXCONN PCEG

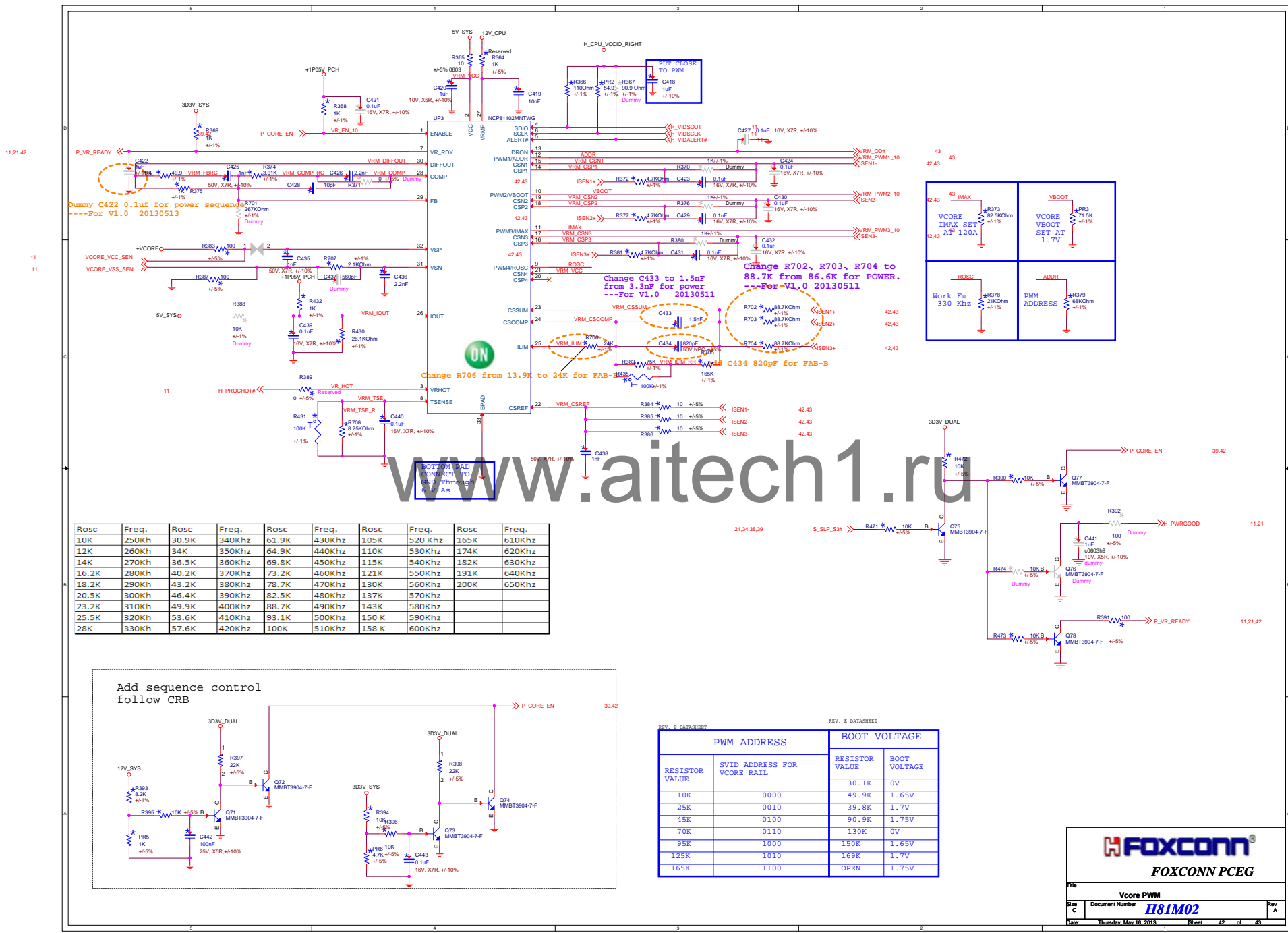
Title			
5V_DUAL/3D3V_DUAL			
Size	Document Number	Rev	
C	H81M02	A	
Date	Thursday, May 16, 2013	Sheet	40 of 43

Max=40A
27A in design guide



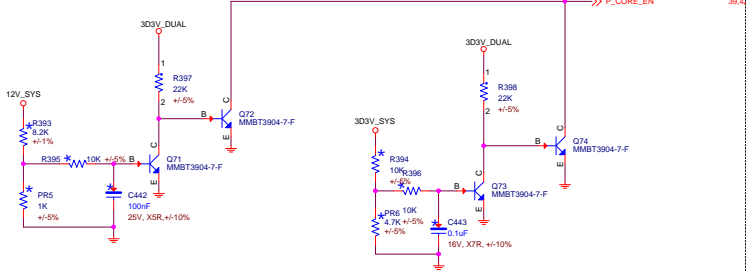
Output voltage: +0.75VRUN +/-5%
Output current: 1.5A





Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.
10K	250Khz	30.9K	340Khz	61.9K	430Khz	105K	520 KHz	165K	610Khz
12K	260Khz	34K	350Khz	64.9K	440Khz	110K	530Khz	174K	620Khz
14K	270Khz	36.5K	360Khz	69.8K	450Khz	115K	540Khz	182K	630Khz
16.2K	280Khz	40.2K	370Khz	73.2K	460Khz	121K	550Khz	191K	640Khz
18.2K	290Khz	43.2K	380Khz	78.7K	470Khz	130K	560Khz	200K	650Khz
20.5K	300Khz	46.4K	390Khz	82.5K	480Khz	137K	570Khz		
23.2K	310Khz	49.9K	400Khz	88.7K	490Khz	143K	580Khz		
25.5K	320Khz	53.6K	410Khz	93.1K	500Khz	150 K	590Khz		
28K	330Khz	57.6K	420Khz	100K	510Khz	158 K	600Khz		

Add sequence control
follow CRB

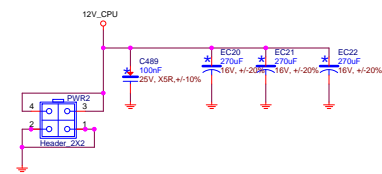
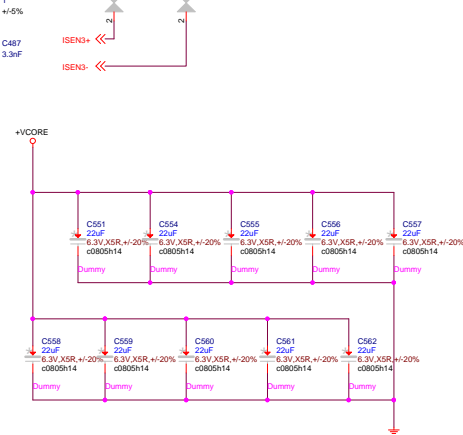
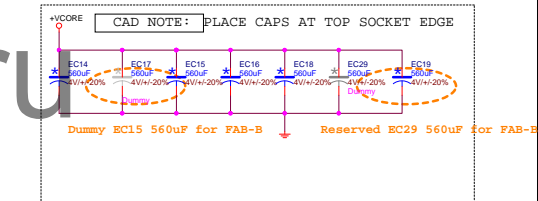
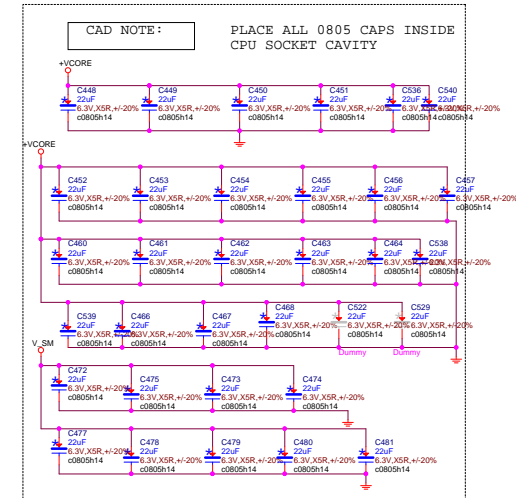
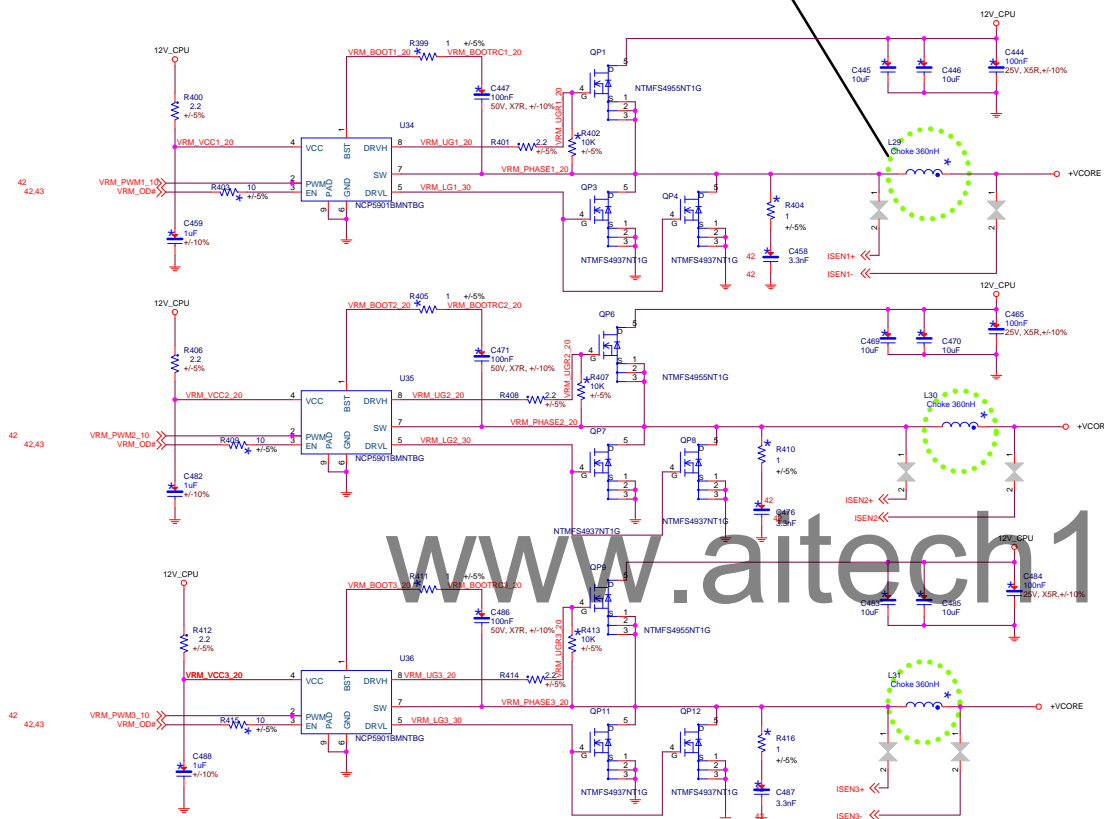


REV. E DATASHEET		REV. E DATASHEET	
PWM ADDRESS		BOOT VOLTAGE	
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	RESISTOR VALUE	BOOT VOLTAGE
10K	0000	30.1K	0V
25K	0010	49.9K	1.65V
45K	0100	39.8K	1.7V
70K	0110	90.9K	1.75V
95K	1000	130K	0V
125K	1010	150K	1.65V
165K	1100	169K	1.7V
		OPEN	1.75V

FOXCONN PCEG

File		
Vcore PWM		
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Change L29,L30,L31
to 363033Y800-VPN-G(CHILISIN and TRIO)
--20130204



File		
Vcore Driver		
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C	H81M02	A
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